FACIT SP1

Facit standard interface for parallel data transfer

Technical description

Part 1

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1 INTRODUCTION

The Facit standard interface for parallel data transfer, designated FACIT SP1, complies with Facit Standard STD 72.721. It is used for character-by-character transfer of data from a source to an acceptor. It also makes provision for limited acceptor-to-source transfers.

The following advantages are among those gained when a standardized interface is adopted:

- Devices can be connected as modules in systems having widely differing configurations without using adaptor units.
- Systems can easily be modified since devices can be added or replaced without difficulty.
- Devices produced by different manufacturers can be connected to each other.
- Devices developed in the future can be connected to existing systems.
- Devices can be developed or modified independently of each other.
- The development of a device can be simplified since the standard specifies how the interface shall be designed both electrically and mechanically. Therefore development time can be shortened.
- Device testing can be simplified since the same test equipment can be used in the developing, manufacturing and servicing of all devices having a standard interface.

The Facit standard interface can be used in widely differing systems and, if necessary, will support sophisticated control. The interface logic is easy to learn. Costs for implementing this standard on a device are low, and as a result it can be used to advantage even on simple devices.

The Facit standard interface resembles the interface specified in British Standard BS 4421:1969 entitled "Specifications for a Digital Input/Output Data Interface for Data Collection Systems". However, the Facit interface makes provision for additional functions and uses fewer signals. Signals having identical functions in the two interfaces have been given the same names in this description as in the BSI Standard.

SP1 defines the interface signals functionally and electrically and presents specifications for the interface connector. ECMA standards or corresponding ISO standards are recommended for the selection of data codes.

The electrical levels in the SP1 are the same as those used for integrated logic circuits designed for a +5 V supply voltage.

2 BRIEF FUNCTIONAL DESCRIPTION

2.1 Signals

Wire No.	Abbreviation	Signal	Direction	Position on 18-pin connector
1	S	Screen	–	A
2	Z	Zero voltage reference	–	B
3	AO	Acceptor Operable	Acceptor to source	C
4	SO	Source Operable	Source to acceptor	D
5	AC	Acceptor Control	Acceptor to source	E
6	SC	Source Control	Source to acceptor	F
7	AM	Acceptor Message	Acceptor to source	H
8	CA	Control Available	Source to acceptor	J
9	–	–	–	K
10	P	Parity bit	Source to acceptor	L
11	D1	Data bit 1	Source to acceptor	M
12	D2	Data bit 2	Source to acceptor	N
13	D3	Data bit 3	Source to acceptor	P
14	D4	Data bit 4	Source to acceptor	R
15	D5	Data bit 5	Source to acceptor	S
16	D6	Data bit 6	Source to acceptor	T
17	D7	Data bit 7	Source to acceptor	U
18	D8	Data bit 8	Source to acceptor	V

Fig. 1

2.2 Description

2.2.1
Data transfer takes place character by character in parallel from source to acceptor.

2.2.2
Data transfer is controlled by signals AO, SO, AC and SC.

2.2.3
AO and SO indicate whether or not the devices are operable.

2.2.4
AC and SC govern data transmission.

2.2.5
D1 through D8, P and CA are data signals. Signal CA provides an indication when the source transfers special control, address or status information to the acceptor using signals D1 through D8.

2.2.6
The acceptor can transfer information of limited scope to the source using signal AM.

2.2.7
Two-way data transmission requires one interface in each direction.

This also applies to one-way data transmission incorporating extensive control or status information sent from acceptor to source.

2.2.8
Data transfer example. See Fig. 3.
NOTE: The effect of line delays is not taken into account in Fig. 3.

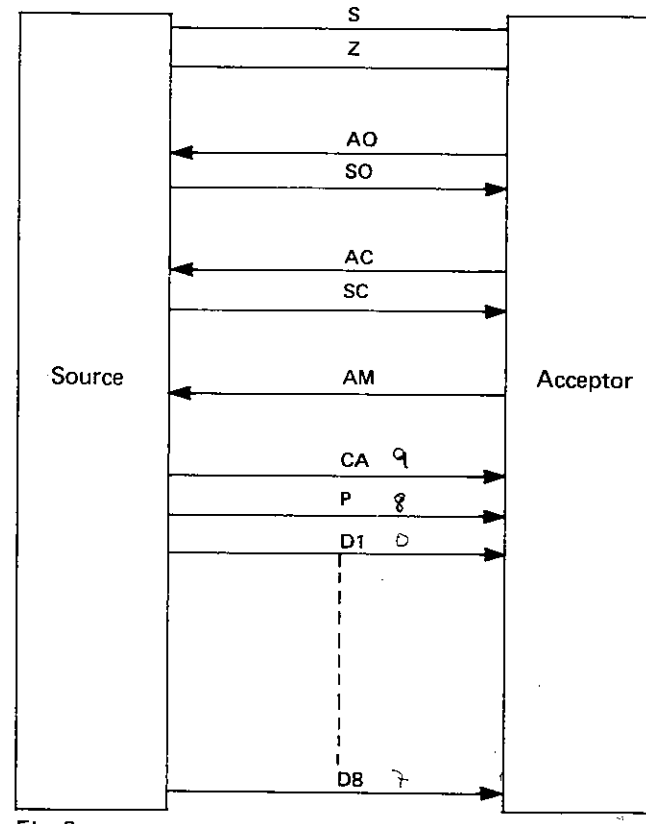

Fig. 2

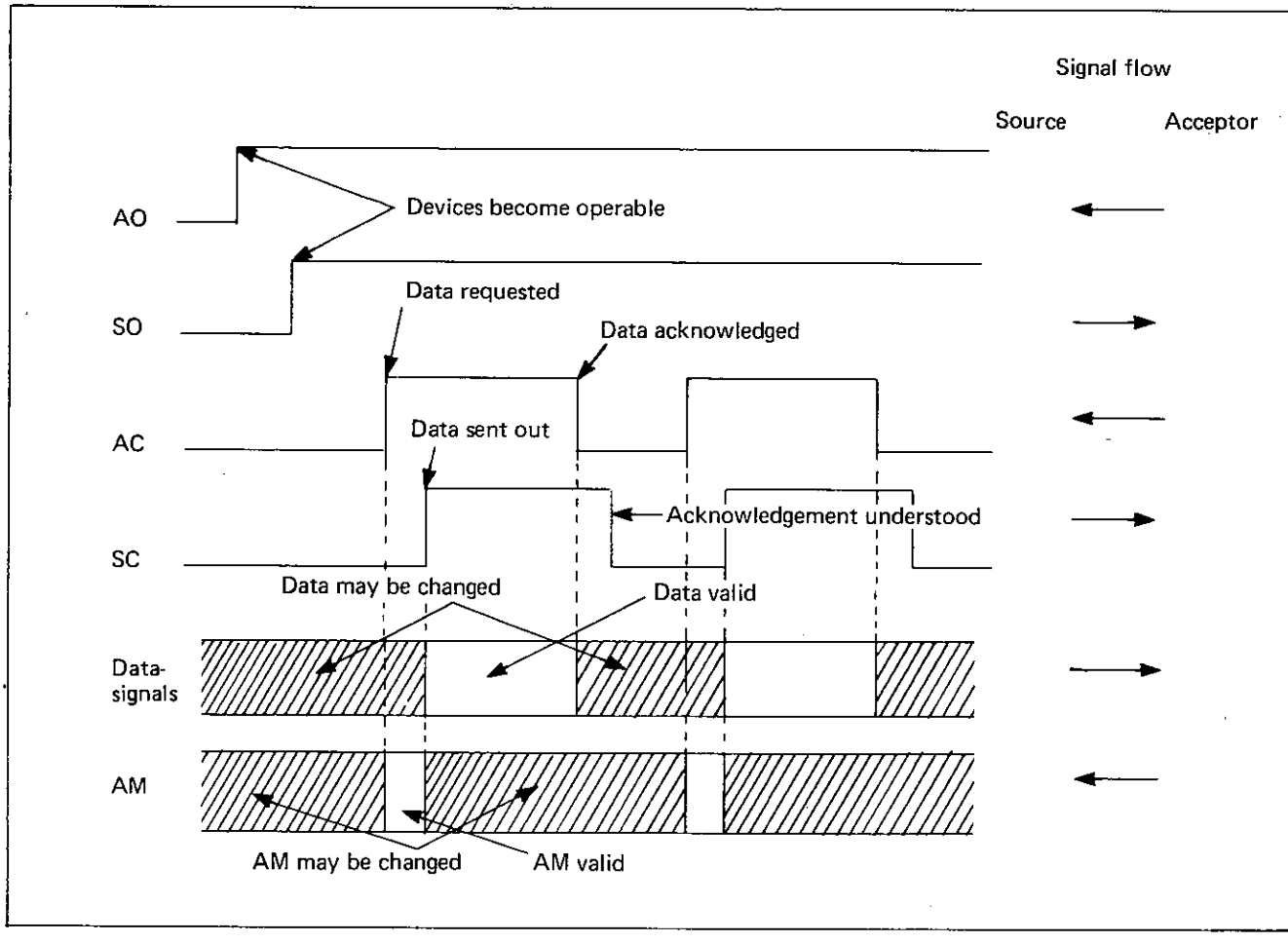

Fig. 3

3 FUNCTIONAL SPECIFICATION

In this specification:
Logic 0 is written 0.
Logic 1 is written 1.
The wires carrying signals D1 through D8, P and CA are referred to as data wires.

3.1 Screen (S)

The cable screen shall be connected to one connector contact, but isolated from the connector body.

A jumper shall be connected between the aforesaid contact and the device chassis, provision shall be made for the jumper to be removed if required.

Note: The device chassis shall be so designed that it can be connected to mains earth if safety regulations so require.

3.2 Zero voltage reference (Z)

The zero voltage reference shall, in each device, be connected directly to the zero voltage point. Each device shall be designed so that the zero voltage point can be connected to its chassis.

3.3 Acceptor Operable (AO)

3.3.1
When the acceptor is operable it shall hold AO at 1.

3.3.2
When the acceptor is not operable, AO shall be 0. In such case, the other acceptor signals are undefined and can assume arbitrary levels. AC shall herewith be considered 0.

3.3.3
AO shall not depend on SO.

3.4 Source Operable (SO)

3.4.1
When the source is operable it shall hold SO at 1.

3.4.2
When the source is not operable, SO shall be 0. In such case, the other source signals are undefined and can assume arbitrary levels. SC shall herewith be considered 0.

3.4.3
SO shall not depend on AO.

3.5 Acceptor Control (AC)

3.5.1
The acceptor shall request information on the data wires by changing AC to 1 after:
(1) it has ascertained that SC is 0,
(2) it is ready to accept information on the data wires and
(3) AM is valid.

3.5.2
The acceptor shall accept the information on the data wires after it has ascertained that SC is 1. It shall then acknowledge the received information by changing AC to 0.

3.6 Source Control (SC)

3.6.1
The source shall change SC to 1 after:
(1) it has ascertained that AC is 1,
(2) it has received AM and
(3) it has sent valid information to the data wires.

3.6.2
The source shall change SC to 0 after it has ascertained that AC is 0.

3.7 Acceptor Message (AM)

3.7.1
At the same time that the acceptor requests new information on the data wires, it can transmit a message to the source using AM. The source shall keep AM at 0 if this signal is not utilized.

3.7.2 AM shall be valid before AC is changed to 1, and shall remain valid until the acceptor has ascertained that SC is 1.

3.8 Control Available (CA)

3.8.1
Normally, the source shall hold CA at 0. When special control, address or status information is transmitted using signals D1 through D8, the source shall hold CA at 1. The source shall hold CA at 0 if this signal is not utilized.

3.8.2
CA shall be valid before SC is changed to 1 and remain valid until the source has ascertained that AC is 0.

3.9 Parity bit (P)

3.9.1
Normally, the source shall generate a parity bit, and it shall be transmitted using signal P. The number of 1s in signals D1 through D8, P and CA shall thus add up to an odd number. If the source does not generate a parity bit, it shall hold P at 0.

3.9.2
P shall be valid before SC is changed to 1 and remain valid until the source has ascertained that AC is 0.

3.10 Data (D1 – D8)

3.10.1
Data shall be transmitted using D1 through D8. D1 shall be used to transmit the least significant bit; lines D2 through D8 shall transmit data in ascending order of significance. Any signals D1 through D8 that are not used shall be held at 0 by the source. ECMA or corresponding standards are recommended for coding D1 through D8 [1].

3.10.2
D1 through D8 shall be valid before SC is changed to 1 and remain valid until the source has ascertained that AC is 0.

3.11 Transfer conditions

3.11.1
The acceptor shall not assume that a fixed amount of time elapses from the instant when the source imparts information to the data wires until the instant when the source changes SC to 1. The acceptor shall thus compensate for the

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1)
7-bit code:
Standard ECMA-6 for a 7-bit Input/Output Coded Character Set
or
ISO/R646 6- and 7-bit Coded Character Sets for Information Processing Interchange.

8-bit code:
The 8-bit code shall comply with the most recent ECMA or ISO recommendation or standard.
At the time of writing – June 1971 – the most recent standard is the ECMA TC1/71/32 Draft ECMA Standard for Extension of the 7-bit Coded Character Set. May 1971.

differences in delays encountered by the different signals in the interconnection cables and in the acceptor receiving circuits.

3.11.2
The source shall not assume that a fixed amount of time elapses from the instant when the acceptor imparts information to the AM wire until the instant when the acceptor changes AC to 1. The source shall thus compensate for differences in delays encountered by the different signals in the interconnecting cables and in the source receiving circuits.

4 INITIAL AND TERMINAL CONDITIONS

4.1 Acceptor

4.1.1
When an acceptor becomes operable, AC shall be defined before AO is changed to 1.

4.1.2
When an acceptor has ascertained that SO is 1, it shall consider SC valid.

4.1.3
If an acceptor changes AO to 0 while AC is 1, it is possible that the source will not have time to receive an AM message (if one was sent).

If an acceptor changes AO to 0 while AC and SC are 1, the source shall not interpret this as an acknowledgement.

Note: For this reason, the acceptor shall be turned off, if possible, only when it is not ready to receive data from the source, i.e. when AC is 0.

4.2 Source

4.2.1
When a source becomes operable, SC shall be defined before the source changes SO to 1.

4.2.2
When a source has ascertained that AO is 1, it shall consider AC valid.

4.2.3
If a source changes SO to 0 while SC is 1, it is possible that the acceptor will not have time to receive the character that was sent.

Note: For this reason, the source shall be turned off, if possible, only when it is not supplying valid information to the data wires, i.e. when SC is 0.

5 ELECTRICAL SPECIFICATION

Voltages and currents affecting the source shall be tested at the source connector sockets.

Voltages and currents affecting the acceptor shall be tested at the acceptor connector pins.

All voltages shall be tested relative to the zero voltage reference.

5.1 Logic levels

5.1.1
Logic 1 shall be represented by a positive voltage. Voltages and currents are specified below in sections 5.2 and 5.3.

5.1.2
Logic 0 shall be represented by a voltage that is close to zero. Voltages and currents are specified below in sections 5.2 and 5.3.

5.2 Signal transmitting circuits

5.2.1
The output voltage from a signal transmitting circuit in the 1 state shall be $\geqslant +2.4$ and $\leqslant +5.5$ V. At + 2.4 V, the output current shall be able to reach 0.4 mA.

5.2.2
The output voltage from a signal transmitting circuit in the 0 state shall be $\geqslant 0$ V and $\leqslant +0.4$ V. At + 0.4 V the input current for D1 through D8, P and CA shall be able to reach 2.0 mA and for AO, SO, AC, SC and AM shall be able to reach 0.2 mA.

5.2.3
The output from a signal transmitting circuit shall be arranged so that it can be short-circuited to an arbitrary contact in the same connector without the circuit being damaged. This shall apply regardless of the logic state of the circuit.

5.2.4
The output from a signal transmitting circuit shall be designed so that it can be left open without the circuit being damaged.

5.3 Signal receiving circuits

5.3.1
Signal receiving circuits for D1 through D8, P, CA and AM shall interpret all voltages $\geqslant +2.0$ V and $\leqslant +5.5$ V as 1. At + 2.4 V the input current shall be $\leqslant 0.4$ mA.

5.3.2
Signal receiving circuits for D1 through D8, P, CA and AM shall interpret all voltages $\geqslant 0$ V and $\leqslant +0.8$ V as 0. At + 0.4 V the output current for D1 through D8, P and CA shall be $\leqslant 2.0$ mA and for AM the output current shall be $\leqslant 0$ mA.

5.3.3
Signal receiving circuits for AM shall interpret an open input as 0.

5.3.4
Signal receiving circuits for AM shall include components that suppress interference.

5.3.5
Signal receiving circuits for AO, SO, AC and SC shall interpret all voltages $\geqslant +2.2$ V and $\leqslant +5.5$ V as 1. At + 2.4 V, the input current shall be $\leqslant 0.4$ mA.

5.3.6
Signal receiving circuits for AO, SO, AC and SC shall interpret all voltages $\geqslant 0$ V and $\leqslant +0.6$ V as 0. At + 0.4 V the output current shall be $\leqslant 0$ mA.

5.3.7
Signal receiving circuits for AO, SO, AC and SC shall exhibit hysteresis $\geqslant 0.3$ V. When the input voltage drops below + 2.2 V, the circuits shall detect changeover from 1 to 0 no earlier than at + 1.9 V and no later than at + 0.6 V. When the input voltage increases above + 0.6 V, the circuits shall detect changeover from 0 to 1 no earlier than at + 0.9 V and no later than at + 2.2 V.

5.3.8
Signal receiving circuits for AO, SO, AC and SC shall interpret an open input as 0.

5.3.9
Signal receiving circuits for AO, SO, AC and SC shall contain components that suppress interference.

5.3.10
The input to a signal receiving circuit shall be designed so that it can be short-circuited to an arbitrary contact in the same connector without the circuit being damaged.

5.3.11
The input to a signal receiving circuit shall be designed so that it can be left open without the circuit being damaged.

6 CONNECTOR SPECIFICATION

6.1 General

6.1.1
The acceptor and source and the cable that joins them shall be provided with a connector complying with this specification.

6.1.2
The connector shall be of the M type as specified in MIL-C-8384 or MIL-C-22857. The connector body shall be designed for 18 signal contacts and 2 guiding elements.

6.1.3
The diameter of the signal contact pins shall be $1.6^{+.01}_{-.04}$ mm.

6.1.4
The nominal diameter of the guide pins shall be 3.2 mm.

6.2 Signal positions

6.2.1
The interface signals shall be assigned positions within the connector as shown in Fig. 4.

6.3 Acceptor connector (plug)

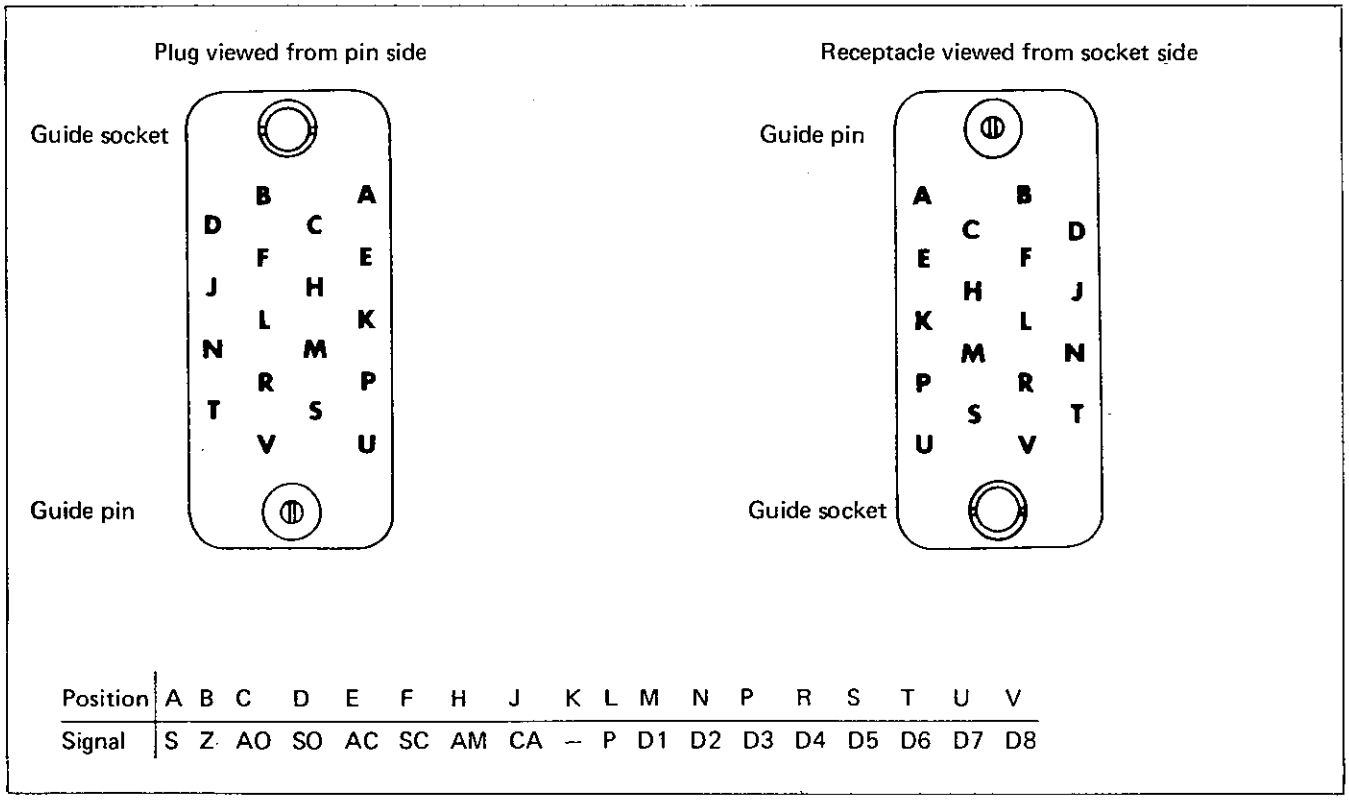
6.3.1
The plug shall comprise a body with pins. Plugs shall be attached to the acceptor and to the end of the cable that plugs into the source.

6.3.2
The guide element adjacent to A in a plug shall be a guide socket.
The guide element adjacent to V in a plug shall be a guide pin.

6.4 Source connector (receptacle)

6.4.1
The receptacle shall comprise a body with sockets. Receptacles shall be attached to the source and to the end of the cable that is connected to the acceptor.

6.4.2
The guide element adjacent to A in a receptacle shall be a guide pin.
The guide element adjacent to V in a receptacle shall be a guide socket.



Position	A	B	C	D	E	F	H	J	K	L	M	N	P	R	S	T	U	V
Signal	S	Z	AO	SO	AC	SC	AM	CA	–	P	D1	D2	D3	D4	D5	D6	D7	D8

Fig. 4

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DATA PRODUCTS DIVISION

AUSTRALIA EAI-Electronics Associates Pty. Ltd., P.O.Box 170, Crows Nest 2065 - AUSTRIA Facit-Addo Verkaufsges.m.b.H., Anschützgasse 31, 1150 Vienna - BELGIUM Facit-Addo S.A., Bettegemlaan 7, 1730 Zellik - BRAZIL Facit S.A., Caixa Postal 30114, 01327 Sao Paulo - CANADA Dometic Canada Ltd., Facit Divisions, P.O.Box 212, Oakville - DENMARK Facit A/S, Lundtoftevej 160, 2800 Lyngby - GREAT BRITAIN Facit-Addo Ltd., Maidstone Road, Rochester - FINLAND OY Facit-Addo AB, P.B. 15, 00101 Helsinki - FRANCE Facit Addo S.A., 308, rue du Prés. S. Allende, 92700 Colombes - HOLLAND Facit Data Products, Postbus 7971, Amsterdam-Buitenveldert - ITALY Facit Data Products S.p.A., Via Pallia 9, 20139 Milano - JAPAN Lindeteves-Jacoberg N.V., I.P.O. Box 5165, Tokyo 100-31 - NORWAY Facit A/S, Postboks 1732, Vika, Oslo - SOUTH AFRICA Garlicks Office Machines, P.O.Box 1057, Johannesburg 2000 - SPAIN Facit Division, Electrolux S.A., Box 627, Madrid - SWEDEN Facit AB, 105 45 Stockholm - SWITZERLAND Facit-Addo AG, Seftigenstrasse 57, 3000 Bern - TAIWAN Syscom, Computer Engineering Co., P.O.Box 48-130, Taipei - USA Facit-Addo Inc., 66 Field Point Road, Greenwich In Conn. 06830 -WEST GERMANY Facit GmbH, Postfach 3008, 4000 Düsseldorf - NEW ZEALAND W & K McLean Ltd., P.O.Box 3097, Auckland

Eng 1.77 Printed in Sweden 77398