NVRAM 15,358 10k JW

GENERAL INSTRUMENT | ER59256

Preliminary Information
August 1983

256 Bit Serial Electrically Erasable and Programmable ROM

Features

- Low cost
- 16x16 serial EEPROM
- Single Supply Operation (5V±10%)
- TTL Compatible
- N-Channel SNOS technology
- Binary addressing
- Word and chip erasable
- 10 years' data retention after 10^4 erase/write cycles per word
- Unlimited read accesses

Description

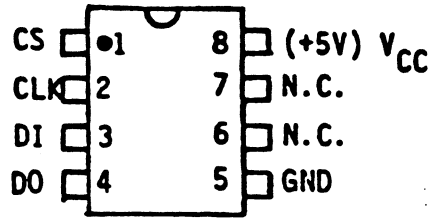
The ER59256 is a low cost, serial EEPROM manufactured in General Instrument's proven SNOS technology. The key features of this device are its +5V only operation and microcomputer compatible architecture. The input (DI) and output (DO) pins may be used separately or may be tied together to form a signle I/O pin. Six 9 bit instructions can be executed. See Table 1. The instruction format has a logical "1" as a start bit, four bits as an op code, and four bits of address. See Table 1. Nonvolatile memory storage is guaranteed for 10 years over the temperature range of 0° to 70°C even after each word of memory has been rewritten up to 10,000 times.

Pin Functions

CS	Chip Select
CLK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	+5V Power Supply
GND	Ground

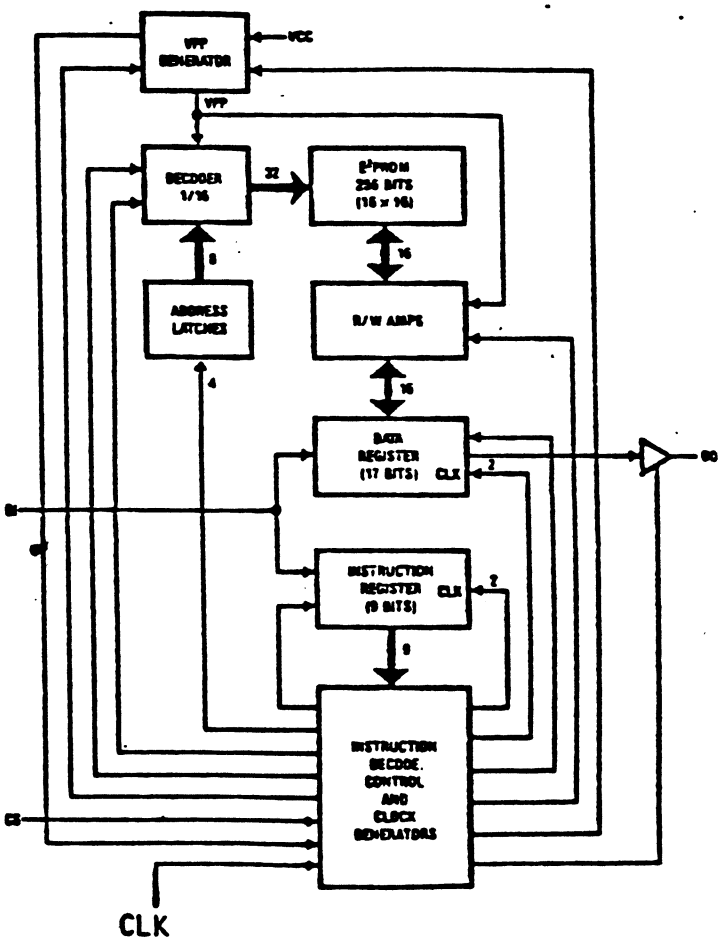
Pin Configuration

8 Pin Dual-in-Line



N.C. = No Internal Connection

Block Diagram



ELECTRICAL CHARACTERISTICS

Maximum Ratings *
All inputs and outputs with respect to ground.....+6V-0.3V
Storage temperature (unpowered and without data retention)...-65°C to 150°C. Soldering temperature of leads (10 seconds).....+300°C.

*Exceeding these ratings could cause permanent damage. Functional operation of this device at these conditions, or any other conditions outside those indicated in the operational sections of this specification, is not implied.

Data labelled "typical" is presented for design guidance only and is not guaranteec

General Instrument makes no warranty, expressed or implied, as to the merchantability or fitness for a particular purpose of this device or its software supplied to the customer.

STANDARD CONDITIONS

(unless otherwise noted)

Vcc = +5 ± 10% volts

= 0 volts

Operating Temperature Range (T_A): 0°C to 70°C

DC CHARACTERISTICS

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
High Level Input Voltage	V_{IH}	2.0	-	Vcc+0.3	V	
Low Level Input Voltage	V_{IL}	-0.3	-	+0.8	V	
High Level Output Voltage	V_{OH}	2.4	-	Vcc	V	I_{OH}=-200µA
Low Level Output Voltage	V_{OL}	-	-	0.4	V	I_{OL}=1.6mA
Input Leakage Current	I_{IL}	-	-	±10	µA	V_{IN}=GND to Vcc
Output Leakage Current	I_{OL}	-	-	±10	µA	V_{OUT}=GND to Vcc
POWER SUPPLY REQUIREMENTS						
Operating Current	Icc2	-	-	10	mA	Vcc=5.5V CS=1
Standby Current	Icc3	-	-	3	mA	Vcc=5.5V CS=0
E/W Operating Current	Icc3	-	-	12	mA	Vcc=5.5V

DC CHARACTERISTICS (continued)

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Consumption (Operating)	Pcc_1	-	-	55	mW	Vcc=5.5V CS=1
Power Consumption (Standby)	Pcc_2	-	-	17	mW	Vcc=5.5V CS=0
Power Consumption (E/W)	Pcc_3	-	-	66	mW	Vcc=5.5V CS=1

AC CHARACTERISTICS

Characteristic	Sym.	Min.	Typ.	Max.	Units	Conditions
Clock Frequency	f_{CLK}	4	-	250	KHZ	
Clock Duty Cycle	D_{CLK}	25	-	75	%	
Chip Select Setup Time	t_{CSS}	0.2	-	-	µs	
Chip Select Hold Time	t_{CSH}	0	-	-	µs	
Data Input Setup Time	t_{DIS}	0.4	-	-	µs	
Data Input Hold Time	t_{DIH}	0.4	-	-	µs	
DO Output Delay (H to L)	t_{PD1}	-	-	2	µs	C_L=100pf
DO Output Delay (L to H)	t_{PD2}	-	-	2	µs	C_L=100pf
Erase/Write Pulse Width	$t_{E/W}$	20	-	30	ms	
Input Capacitance	C_I	-	-	6	pf	V_{IN}=0V
Output Capacitance	C_O	-	-	10	pf	V_{OUT}=0V

0-15 Adress

See Figur 2

Instruction	SB	Op Code	Address	Data	Comments
READ	1	~~0100~~ 1000	A3A2A1A0		Read register A3A2A1A0
WRITE	1	0100	A3A2A1A0	D15-D0	Write register A3A2A1A0
ERASE	1	1100	A3A2A1A0		Erase register A3A2A1A0
EWEN 'EN	1	0011	0000		Erase/write enable
EWDS	1	0000	0000		Erase/write disable
ERAL	1	0010	0000		Erase all registers

4

16bits register

Table 1 Instruction Set

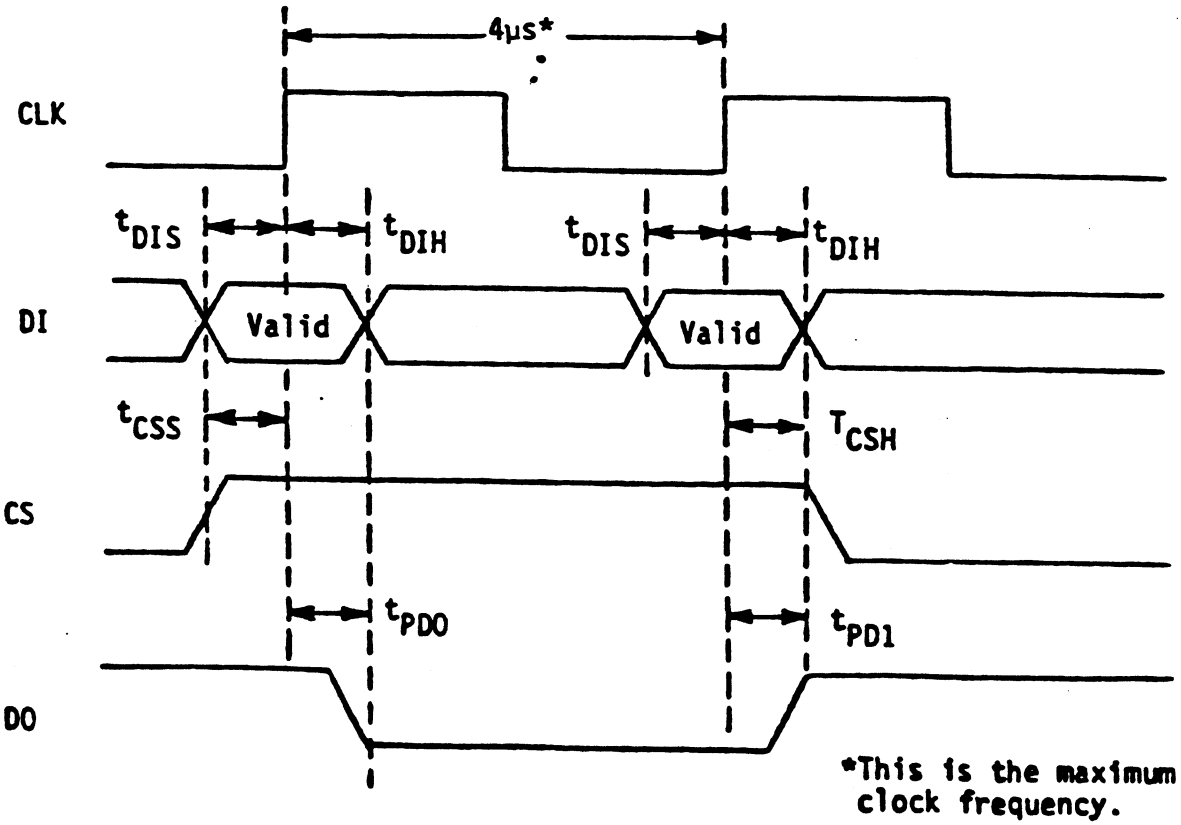
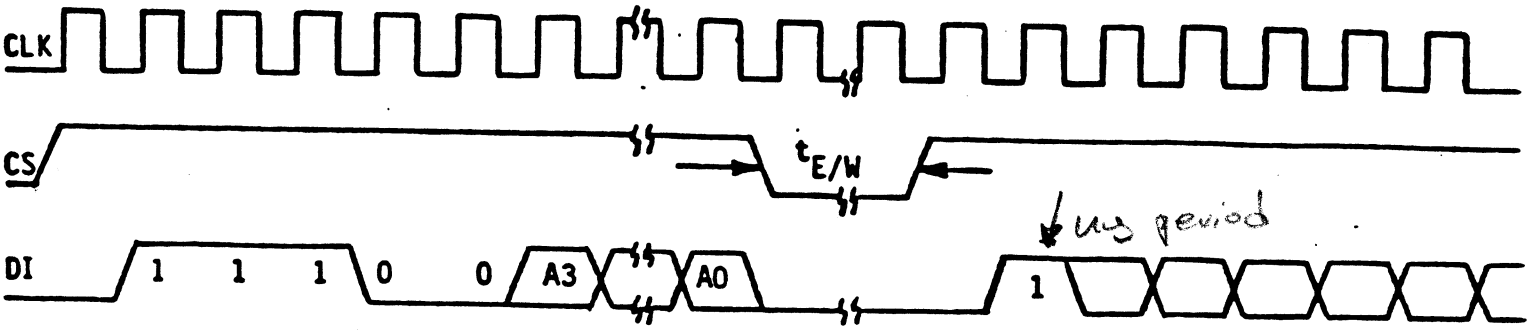
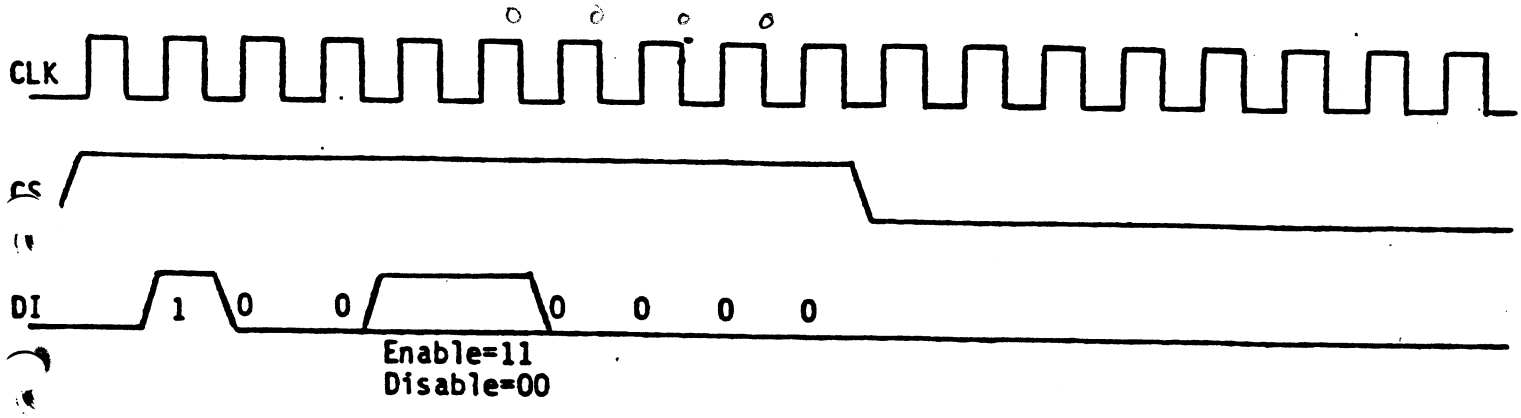


Figure 1. Synchronous Data Timing



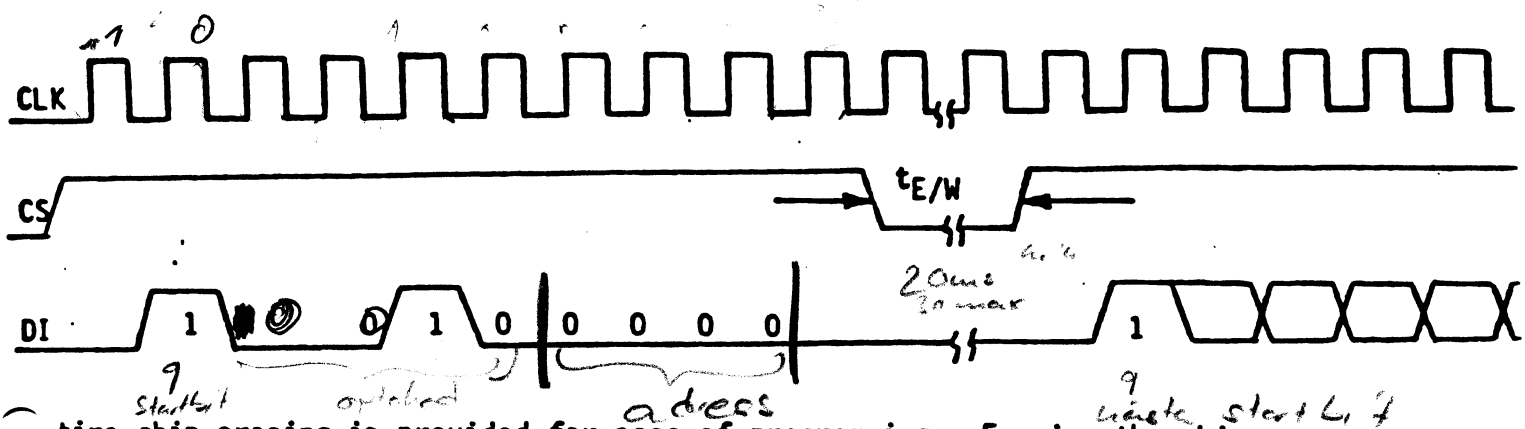
Like most E^2PROMS, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at lease one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

Figure 4. Erase Mode



Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

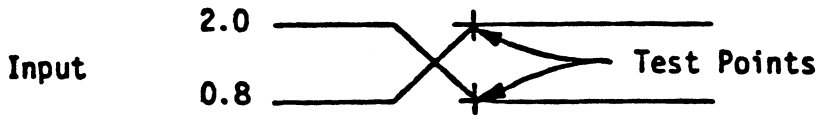
Figure 5. Erase/Write Enable and Disable

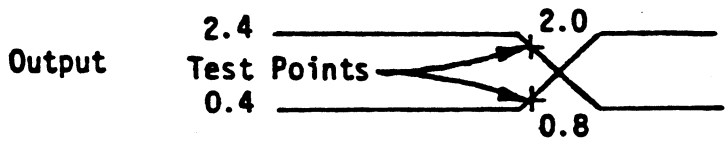


tire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

Figure 6. Chip Erase Mode

A.C. Testing, Input and Output Waveforms

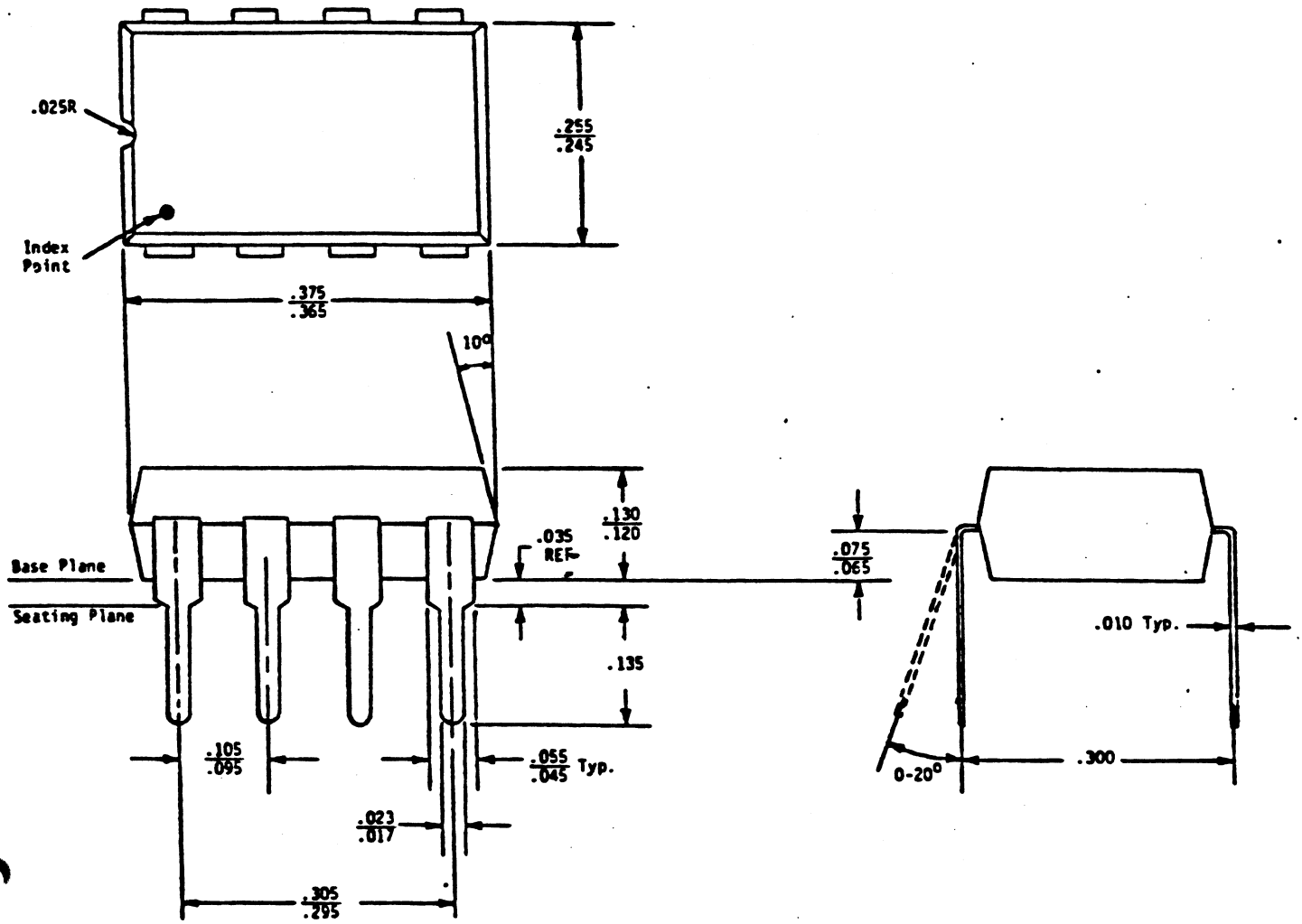


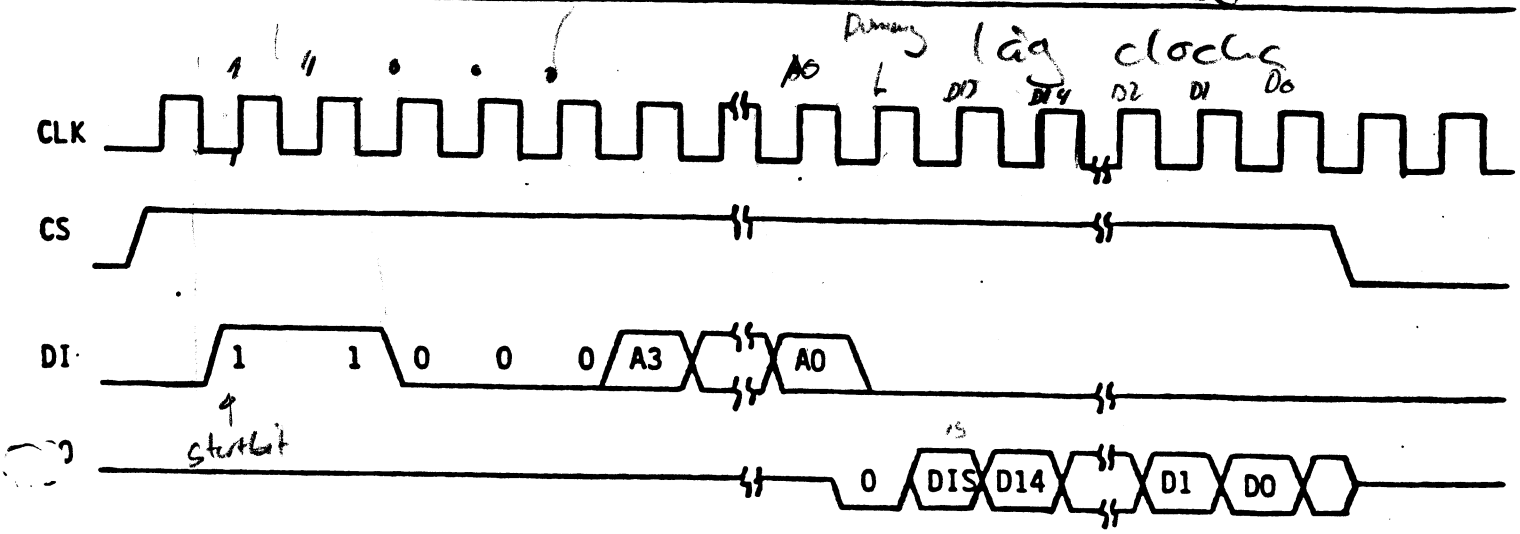


A.C. Testing: Inputs are driven at 2.0V for an input logic high and 0.8V for an input logic low. Timing measurements of the output waveforms are made at 2.0V for an output logic high and 0.8V for an output logic low.

PACKAGE OUTLINE

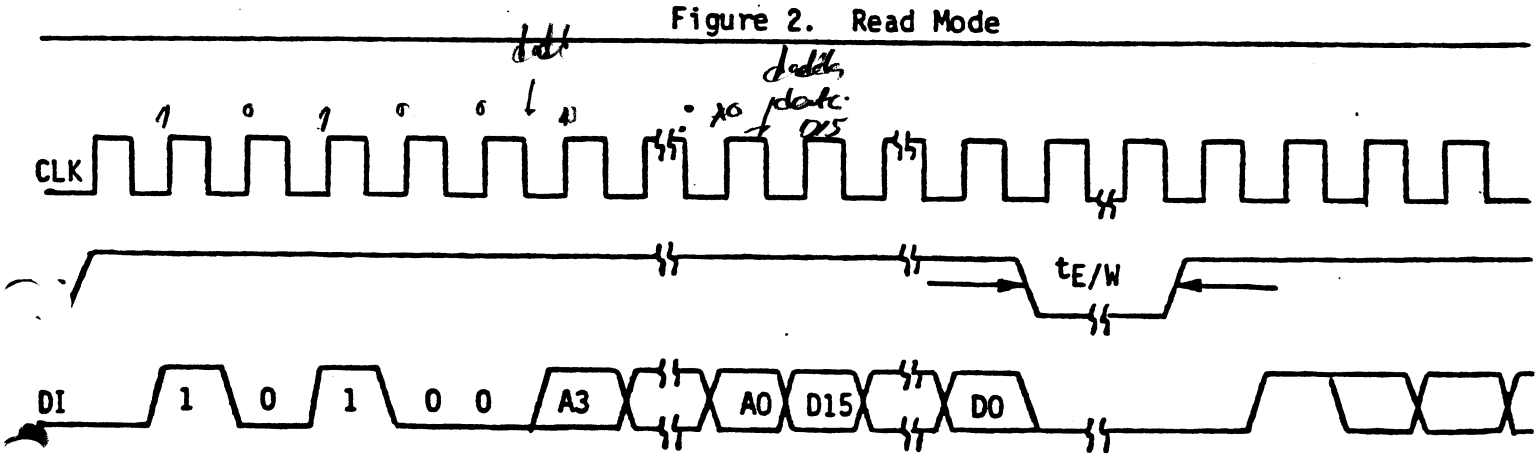
8 Lead Dual-in-Line (All dimensions are in inches)





The READ instruction is the only instruction which outputs serial data on the DO pin. Only during the READ mode is the output pin (DO) valid. During all other modes the DO pin is in tri-state, eliminating bus contention. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical "0") precedes the 16-bit data output string. The output data changes during the high state of the system clock.

Figure 2. Read Mode



The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes which prevents spurious programming during other modes. When CS rises to V_{IH}, the programming cycle ends. All programming modes should be ended with CS high for one clock period, or followed by another instruction.

Figure 3. Write Mode