GENERAL INSTRUMENT	AY9229/9229B/ 9229T/9229BT

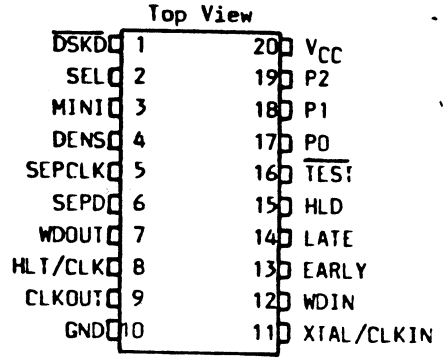
FLOPPY DISK INTERFACE CIRCUIT

FEATURES:

- Digital Data Separator which performs complete data separation function for floppy disk drives
  Separates FM and MFM encoded data
- No critical adjustments necessary
- Variable Write Precompensation
- Internal Crystal Oscillator Circuit
- Track-Selectable Write Precompensation
- Retriggerable Head-Load Timer
- 5 1/4" and 8" compatible
- Compatible with the 179X, 765, and other standard Floppy Disk Controllers
- General Instrument N-channel MOS Technology
- Single +5 Volt Supply
- TTL Compatible

PIN CONFIGURATION
20 LEAD DUAL IN LINE

Top View

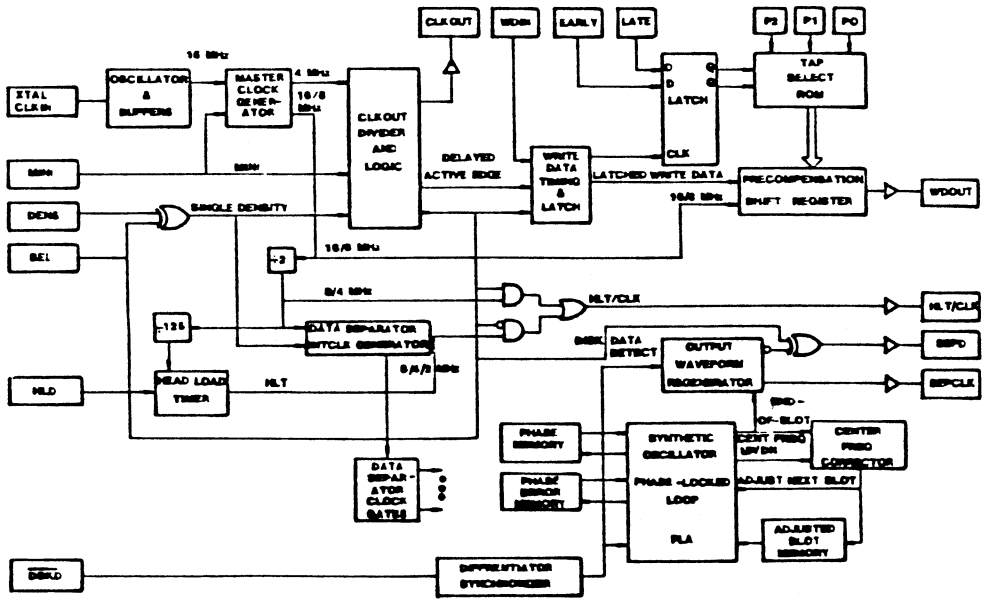


FUNCTIONAL DESCRIPTION

The AY9229/B is an N-channel silicon gate integrated circuit designed to complement either the 179X or 765 (8272) type of floppy disk controller chip. It incorporates a digital data separator, write precompensation logic, and a head-load timer. The AY9229/B can be configured to work with either the 179X or 765 type of controller through the use of the SEL pin. The AY9229/B provides a number of different dynamically selected precompensation values to allow different values to be used when writing to the inner and outer tracks of the floppy disk drive.

The AY9229/B operates from a +5V supply and simply requires that a 16 or 8 MHz crystal (AY9229/B) or TTL-level clock be connected to the XTAL/CLKIN pin (AY9229T/BT). All inputs and outputs are TTL compatible. (The AY9229/T are intended for 5 1/4" disks and the AY9229B/T for 5 1/4" and 8" disks).

FIGURE 1 AY9229 BLOCK DIAGRAM



DESCRIPTION OF PIN FUNCTIONS

PIN NO.	SYMBOL	I/O	DESCRIPTION
1	$\overline{\text{DSKD}}$	I	This input is the raw read data received from the drive. (This input is active low.)
2	SEL	I	This input signal, when low, programs the AY9229/B for a 179X type of LSI controller. When SEL is high, the AY9229/B is programmed for a 765 (8272) type of controller. (See Figure 5).
3	MINI	I	The state of this input determines whether the AY9229/B is configured to support 8" or 5 1/4" floppy disk drive interfaces. It is used in conjunction with the DENS input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency, the precompensation value, the head load delay time (when in 179X mode) and the HLT/CLK frequency (when in 765 modes). (See Figures 3, 4, and 5).
4	DENS	I	The state of this input determines whether the AY9229/B is configured to support single density (FM) or double density (MFM) floppy disk drive interfaces. It is used in conjunction with the MINI input to prescale the clock for the data separator. The state of this input also alters the CLKOUT frequency when in the 765 mode. (See Figures 3, 4, and 5).
5	SEPCLK	O	A square-wave window clock signal output derived from the $\overline{\text{DSKD}}$ input.
6	SEPD	O	This output is the regenerated data pulse derived from the raw data input ($\overline{\text{DSKD}}$). This signal may be either active low or active high as determined by SEL (pin 3).
7	WDOUT	O	The precompensated WRITE DATA stream to the drive.
8	HLT/CLK	O	When in the 765 mode (SEL high), this output is the master clock to the floppy disk controller. When in the 179X mode, this signal goes high after the head load delay has occured following the HLD input going high. This output is retriggerable. (See Figure 4).
9	CLKOUT	O	This signal is the write clock to the floppy disk controller. Its frequency is determined by the state of the MINI, DENS, and SEL input pins. (See Figure 4).
10	GND		Ground.
11	XTAL/CLKIN	I	This input is for direct connection to a 16 MHz or 8 MHz crystal (AY9229/B only). The other pin of the crystal is grounded. XTAL/CLKIN may alternatively be connected to a single-phase TTL-level clock. The AY9229T and BT require an external TTL-level clock.

DESCRIPTION OF PIN FUNCTIONS (continued)

PIN NO.	SYMBOL	I/O	DESCRIPTION
12	WDIN	I	The write data stream from the floppy disk controller.
13	EARLY	I	When this input is high, the current WRITE DATA pulse will be written early to the disk.
14	LATE	I	When this input is high, the current WRITE DATA pulse will be written late to the disk. When both EARLY and LATE are low, the current WRITE DATA pulse will be written at the nominal position.
15	HLD	I	This input is only used in 179X mode. A high level at this input causes a high level on the HLT/CLK output after the specified head-load time delay has elapsed. The delay is selected by the state of the MINI output. (See Figure 4).
16	$\overline{TEST}$	I	This input (when low) decreases the head-load time delay and initializes the data separator. This pin is for test purposes only. This input has an internal pull-up resistor and should be tied high or disconnected for normal operation.
17	P0	I	
18	P1	I	P2-P0 select the amount of precompensation applied to the write data. (See Figure 3).
19	P2	I	
20	V_{CC}		+5 VOLT SUPPLY

OPERATION

Data Separator

The XTAL/CLKIN input clock is internally divided to provide an internal clock. The division ratio is selected by the SEL, MINI and DENS inputs depending on the type of drive used. (See Figure 2).

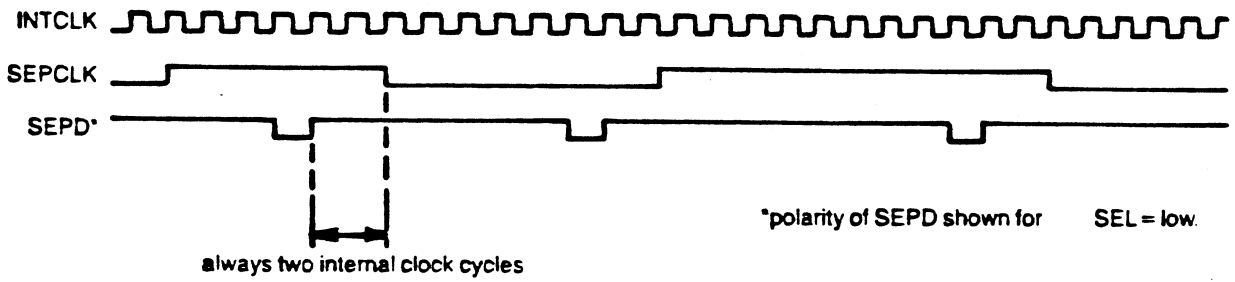
The AY9229/B detects the leading (negative) edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPCLK output.

Separate short- and long-term timing correctors assure accurate clock separation.

The SEPCLK frequency is nominally 1/16 the internal clock frequency. Depending on the internal timing correction, the duration of any SEPCLK half-cycle may vary from a nominal of 8 to a minimum of 6 and maximum of 11 internal clock cycles.

FIGURE 2

INPUTS			DIVISOR
SEL	DENS	MINI	f(XTAL/CLKIN)/f(INTCLK)
0	0	0	2
0	0	1	4
0	1	0	4
0	1	1	8
1	0	0	4
1	0	1	8
1	1	0	2
1	1	1	4



Precompensation

The desired precompensation delay is determined by the state of the inputs P0, P1 and P2, per Figure 3. Logic levels present on these pins may be changed dynamically as long as the inputs are stable during the time the floppy disk controller is writing to the drive and the inputs meet the minimum setup time with respect to the write data from the floppy disk controller.

MINI	P2	P1	P0	PRECOMP VALUE
0	0	0	0	0 ns
0	0	0	1	62.5 ns
0	0	1	0	125 ns
0	0	1	1	187.5 ns
0	1	0	0	250 ns
0	1	0	1	250 ns
0	1	1	0	312.5 ns
0	1	1	1	312.5 ns

FIGURE 3

WRITE PRECOMPENSATION VALUE SELECTION

MINI	P2	P1	P0	PRECOMP VALUE
1	0	0	0	0 ns
1	0	0	1	125 ns
1	0	1	0	250 ns
1	0	1	1	375 ns
1	1	0	0	500 ns
1	1	0	1	500 ns
1	1	1	0	625 ns
1	1	1	1	625 ns

NOTE:

All values shown are obtained with a 16 MHz reference clock. Multiply precompensation values by two for 8 MHz operation.

OPERATION (continued)

Head Load Timer

The head load delay is either 40 ms or 80 ms, depending on the state of MINI. (See Figure 4). The purpose of this delay is to ensure that the head has enough time to engage properly. The head load timer is only used in the 179X mode; it is non-functional in the 765 mode.

The 179X initiates the loading of the floppy disk drive head by setting HLD high. The controller then waits the programmed amount of time until the HLT signal from the AY9229/B goes high before starting a read or write operation.

FIGURE 4

CLOCK AND HEAD LOAD TIME DELAY SELECTION

INPUTS			OUTPUTS	
SEL	DENS	MINI	CLKOUT	HLT/CLK
0	0	0	2 MHz	40 ms
0	0	1	1 MHz	80 ms
0	1	0	2 MHz	40 ms
0	1	1	1 MHz	80 ms
1	0	0	500 KHz	8 MHz
1	0	1	250 KHz	4 MHz
1	1	0	1 MHz	8 MHz
1	1	1	500 KHz	4 MHz

NOTE: All values shown are obtained with a 16 MHz reference clock. Divide all frequencies and multiply all periods by two for 8 MHz operation.

FIGURE 5

FLOPPY DISK DRIVE AND CONTROLLER SELECTION

INPUTS			FLOPPY DISK	FLOPPY DISK	FLOPPY DISK
SEL	DENS	MINI	DRIVE TYPE	DRIVE DENSITY	CONTROLLER TYPE
0	0	0	8" DRIVE	DOUBLE	179X
0	0	1	5 1/4" DRIVE	DOUBLE	179X
0	1	0	8" DRIVE	SINGLE	179X
0	1	1	5 1/4" DRIVE	SINGLE	179X
1	0	0	8" DRIVE	SINGLE	765 (8272)
1	0	1	5 1/4" DRIVE	SINGLE	765 (8272)
1	1	0	8" DRIVE	DOUBLE	765 (8272)
1	1	1	5 1/4" DRIVE	DOUBLE	765 (8272)

ELECTRICAL CHARACTERISTICS

Maximum Guaranteed Ratings*

Operating Temperature Range..... 0°C to +70°C
Storage Temperature Range..... -55°C to +150°C
Positive Voltage on any I/O Pin, with respect to ground..... +8.0V
Negative Voltage on any I/O Pin, with respect to ground..... -0.3V
Power Dissipation..... 0.75W

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied - operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (Unless otherwise noted)
T_A = 0°C to 70°C, V_{CC} = 5V ± 5%

DC CHARACTERISTICS

Characteristic	Sym	Min	Typ	Max	Unit	Conditions
INPUT VOLTAGE						
Low Level	V_{IL}	-0.3	-	0.8	V	Except XTAL/CLKIN
High Level	V_{IH}	2.0	-	(V_{CC})	V	
XTAL/CLKIN INPUT VOLTAGE						
AC Amplitude	-	1.0	-	-	V_{PP}	XTAL/CLKIN only; input is
Instantaneous voltage	-	-0.3	-	(V_{CC})	V	AC-coupled.
OUTPUT VOLTAGE						
Low Level	V_{OL}	-	-	0.4	V	I_{OL} = 1.6mA except HLT/CLK
						I_{OL} = 0.4mA, HLT/CLK only
High Level	V_{OH}	2.4	-	-	V	I_{OH} = -100μA, HLT/CLK
						I_{OH} = -400μA, HLT/CLK only
POWER SUPPLY CURRENT	I_{CC}	-	-	100	mA	
INPUT LEAKAGE CURRENT	I_{IL}	-	-	10	μA	V_{IN} = 0 to V_{CC}
INPUT CAPACITANCE	C_{IN}	-	-	10	pF	Except CLKIN
	-	-	-	25	pF	CLKIN only

AC CHARACTERISTICS

(Assumes XTAL/CLKIN = 16 MHz unless otherwise specified)

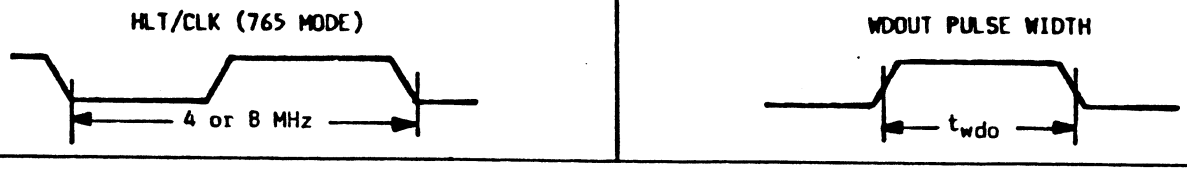
Characteristic	Sym	Min	Typ	Max	Unit	Conditions
XTAL/CLKIN FREQUENCY	-	3.95	16	16.2	MHz	AY9229B
	-	3.95	8	8.1	MHz	AY9229
L/CLKIN DUTY CYCLE	T_{clkoh}	25	-	75	%	
		465	500	515	ns	SEL = low; MINI = high
		215	250	265	ns	SEL = low; MINI = low
		90	125	140	ns	SEL = high
	T_{wdo}	280	312.5	350	ns	
	T_d	50	-	400	ns	
	T_{dNEC}	0	-	400	ns	
	T_{wdE}	-	562.5	-	ns	
	T_{wdN}		precomp value			See Figure 3
	T_{wdL}		2 x precomp value			See Figure 3
	T_s	1.0	-	-	μs	

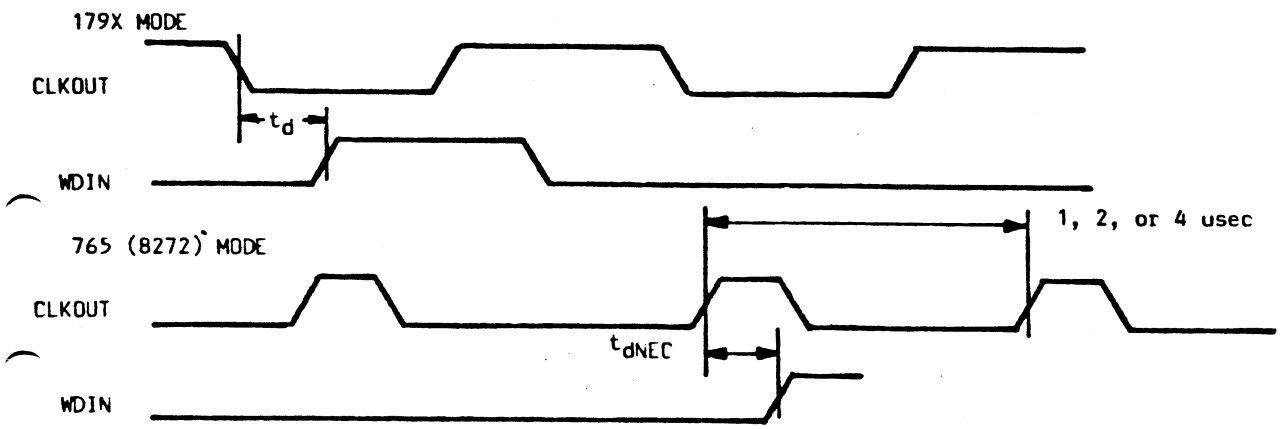
CRYSTAL SPECIFICATIONS

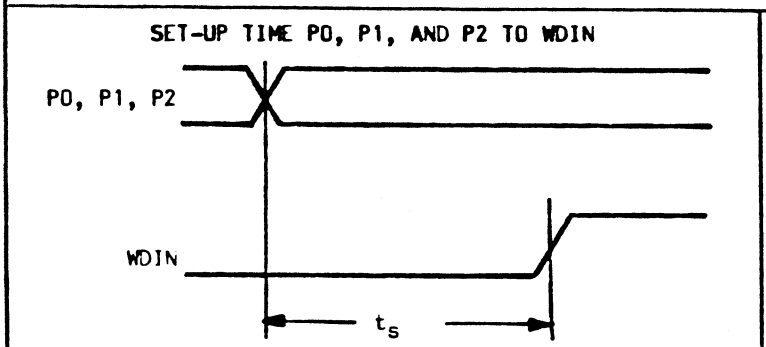
Frequency (8" Disk Drive) 16 MHz, at Cut
(5 1/4" Disk Drive) 8 MHz, at Cut
Holder Preferred HC - 18/V

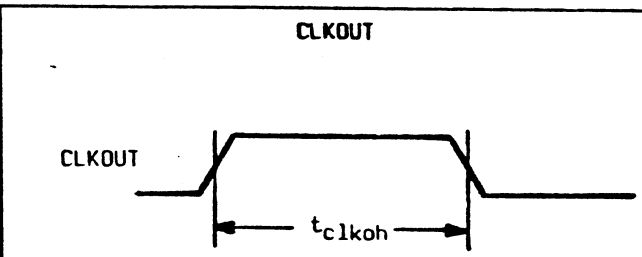
Frequency and stability tolerance ±.05% from 0°C to 70°C
Series Resistance 50 ohm max

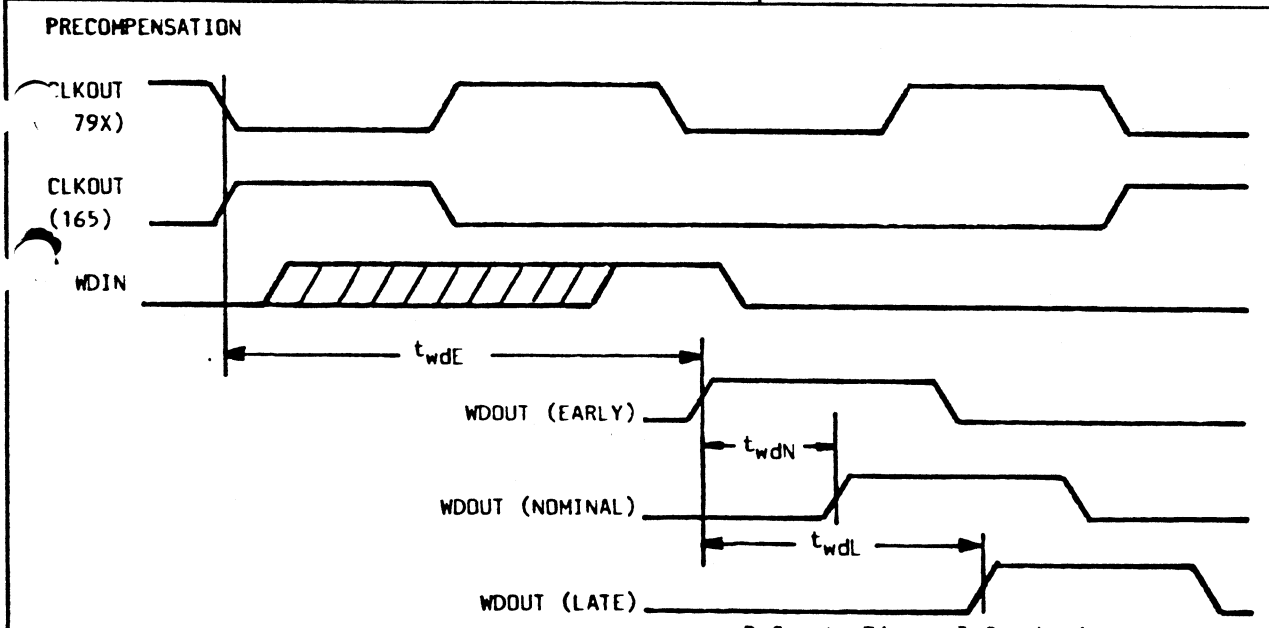
FIGURE 6 AC TIMING CHARACTERISTICS





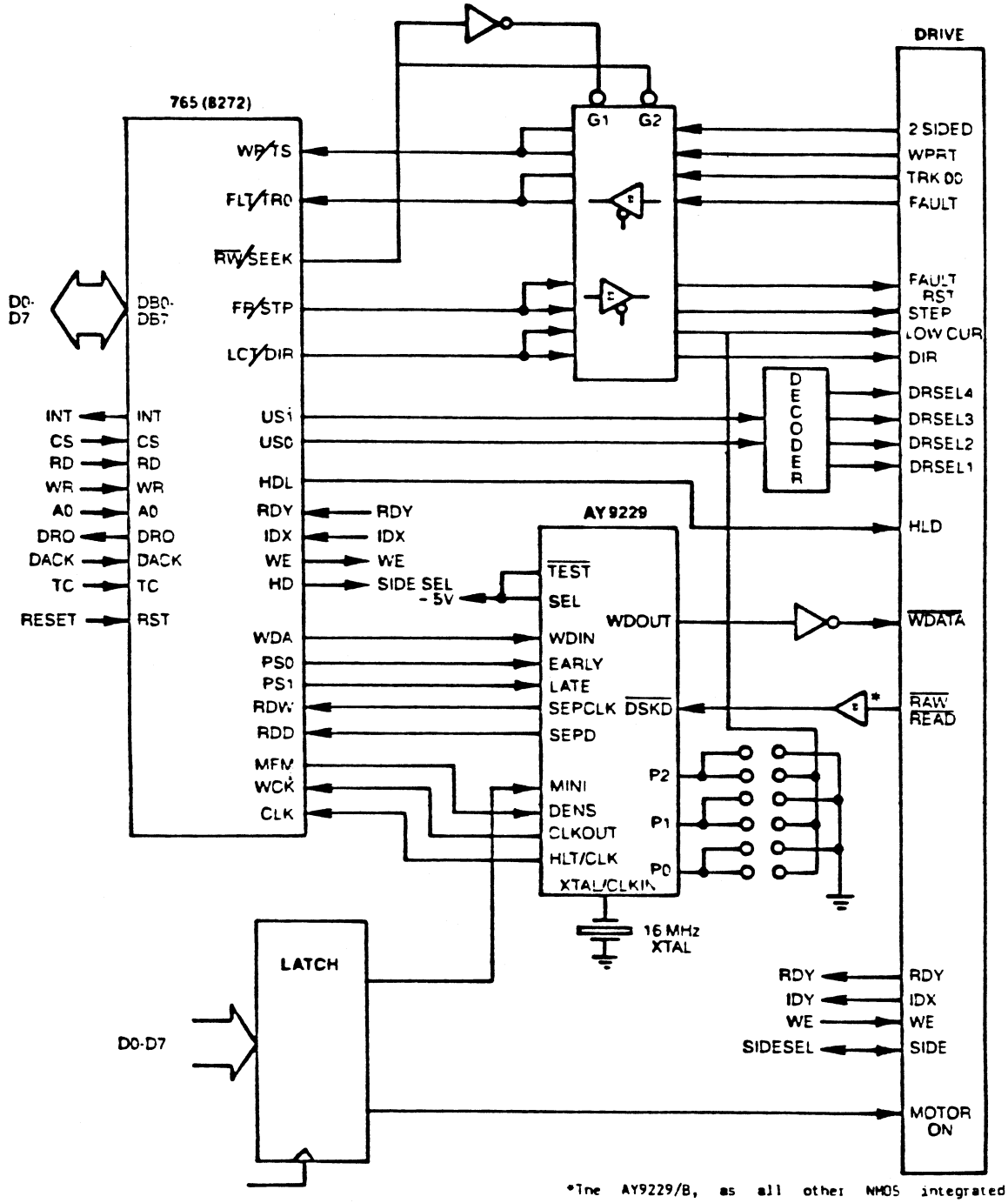






Refer to Figure 3 for t_p (precompensation) value.

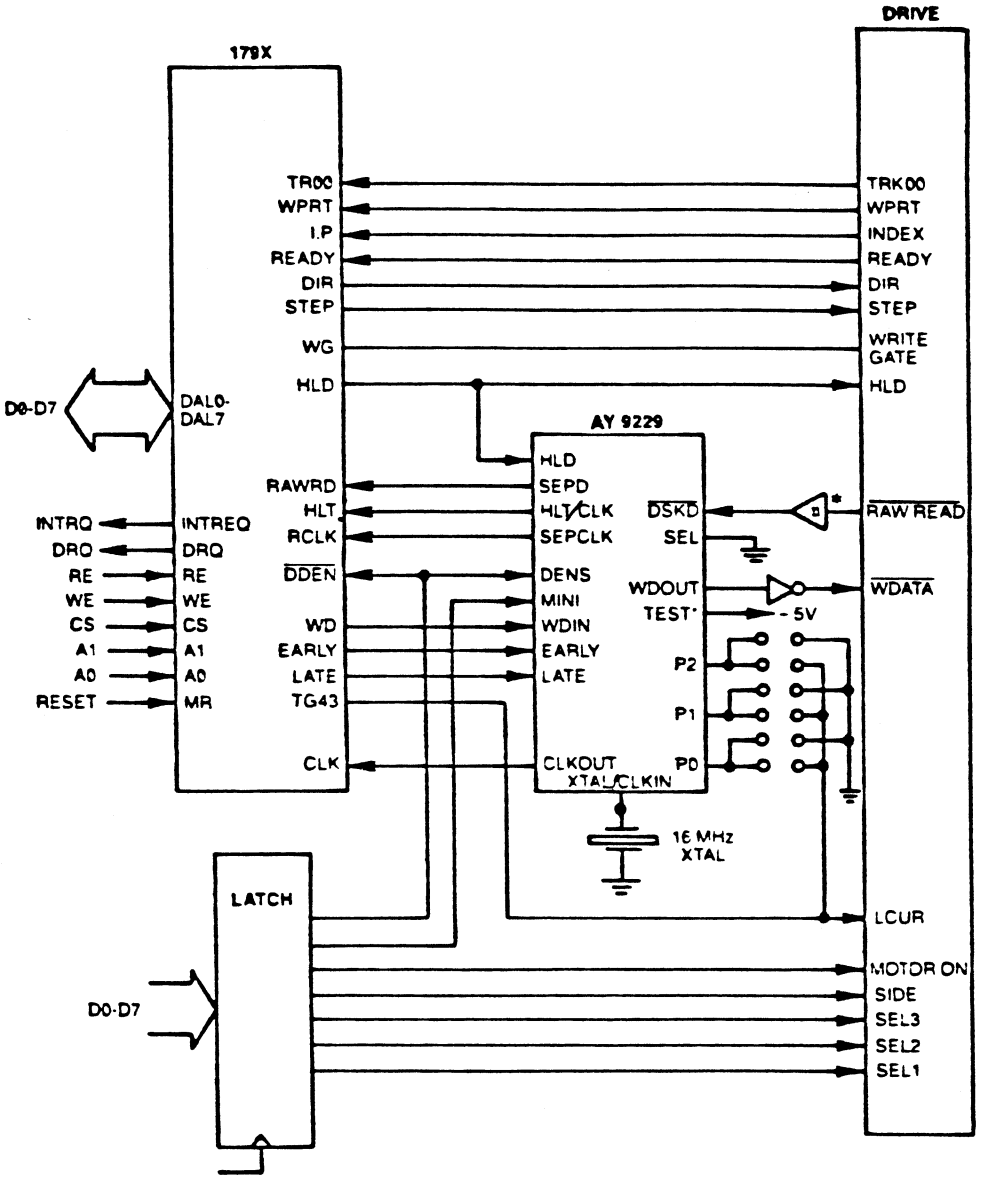
FIGURE 7 TYPICAL SYSTEM IMPLEMENTATION - 765 (8272)



*The AY9229/B, as all other NMOS integrated circuits, presents a high impedance on all inputs.

To avoid soft errors caused by transmission line effects and noise where there is long cabling between the floppy disk drive and the controller board, the use of a (non-inverting) TTL schmidt-trigger input gate or bus transceiver is recommended at the $\overline{DSKD}$ input to the AY9229/B.

FIGURE 8 TYPICAL SYSTEM IMPLEMENTATION - 179X



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