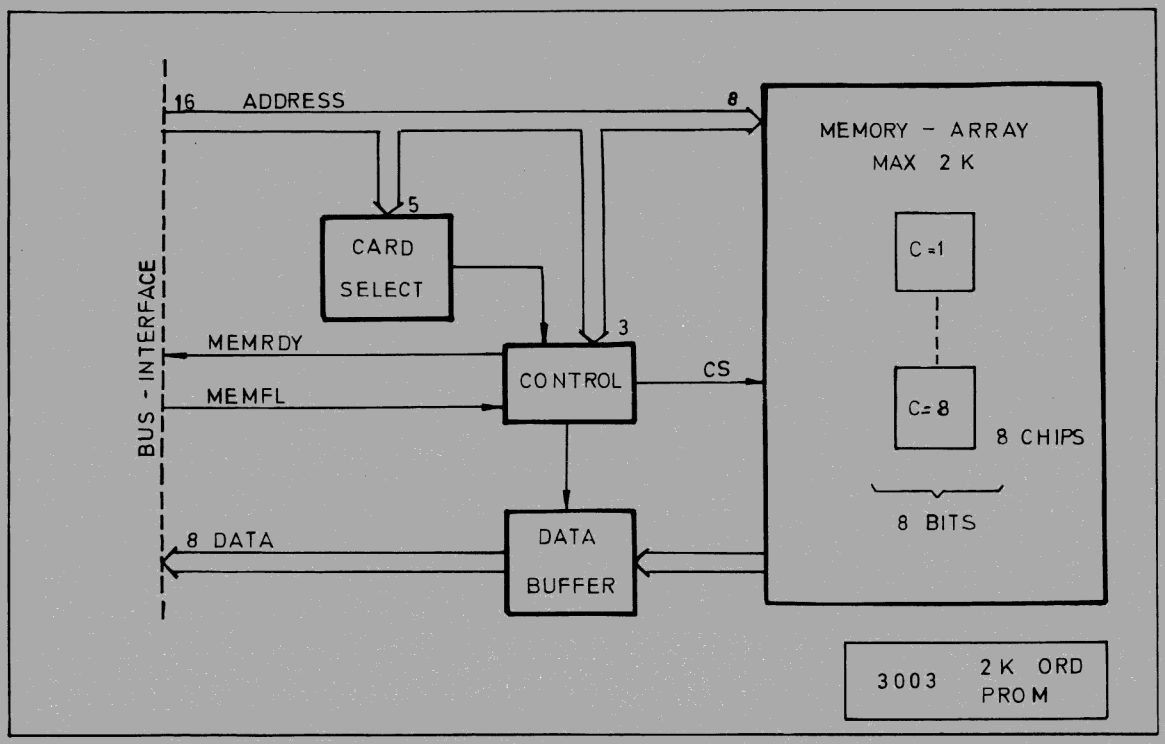
DATABOARD 4680

2K ORD PROM

3003



BESKRIVNING

3003 är ett raderbart PROM som baserats på minneskrets 1702A.

– Det bestyckas av användaren

  Detta sker i steg av 256 bytes (256 x 8 bitar per kapsel)

– Det läggs valfritt inom 64K med multipel av 2K.

  Adressval sker med byglingsplugg

Kortet uppfyller bussnormerna för last– och drivförmåga i DataBoard 4680

SATTCO AB · DALVÄGEN 10 · 171 36 SOLNA · TFN 08/83 02 80

TEKNISKA DATA:

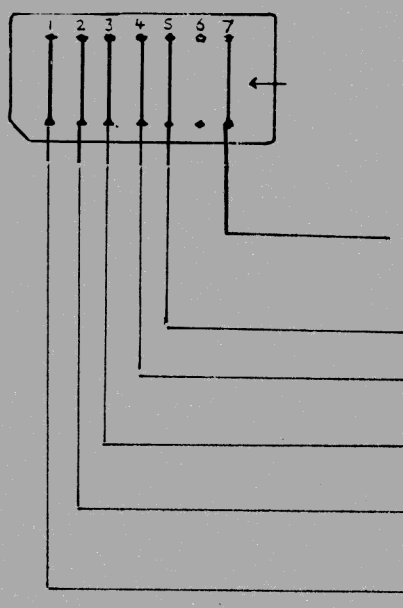
– Matningsspänning:	+ 5V ± 5% –12V ± 5%
– Strömförbrukning fullt bestyckad:	+ 5V – 520 mA –12V –
– Accesstid:	Nominellt 1 /usek
– Mått:	Enkelt europakort 100 x 160 mm
– Kontakt:	B 64 pol. tvåradigt europadon (41612)

KONTAKTNUMRERING: Se systembeskrivningen

SIGNALER mellan CPU och PROM–kortet:

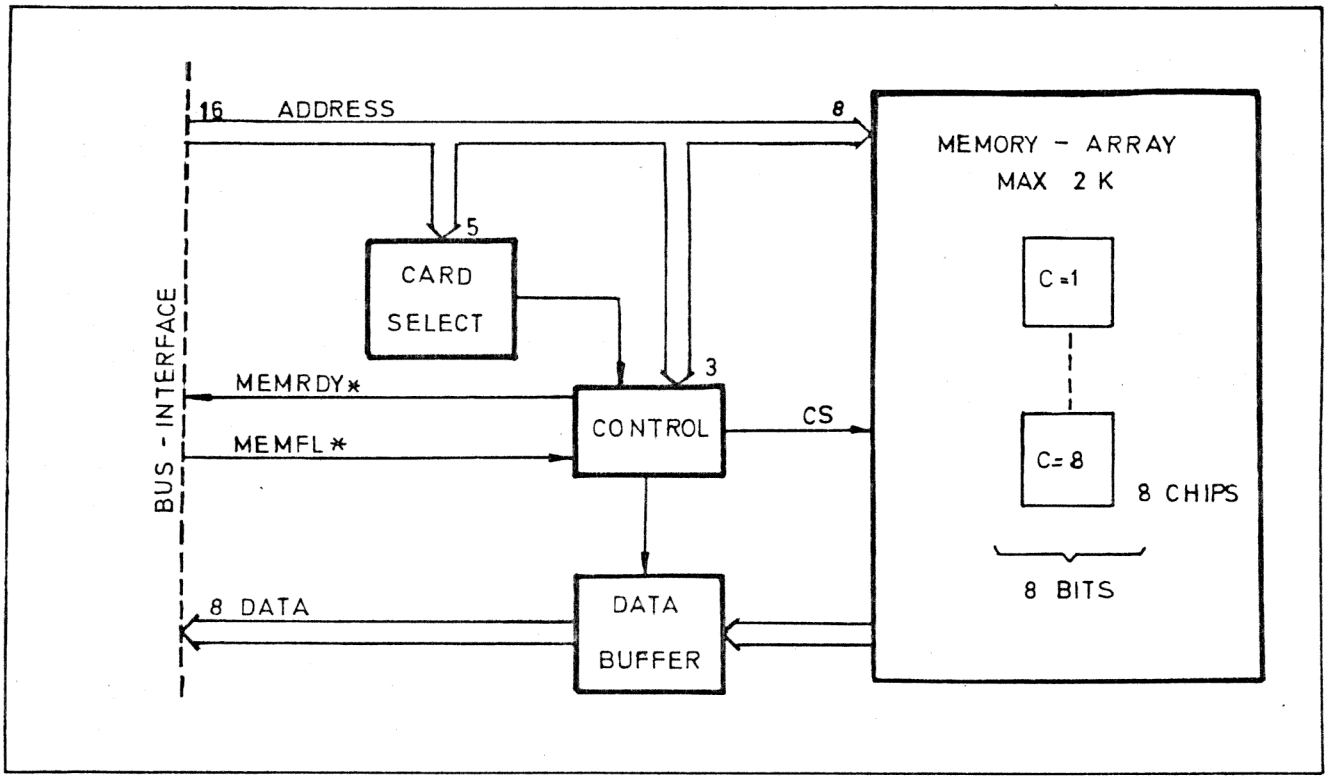
- 16 bitars adressbuss
- 8 bitars tristate databuss
- MEMRDY är konstruerad för att begära två "wait–states"
- "MEM control" innehåller signalen MEMFL för läsning

BYGLINGAR: Val av minnets placering inom 64K görs med byglingsplugg.



Exempel: "1" och "3" klippta ger (2 + 8 = 10) minnesplacering 10 – 12K

Jan 79



DESCRIPTION

3003 is a memory module for erasable PROM

- Memory circuit type 1702A.
- Memory capacity 2 kbytes.
- The memory circuits are included by the user. It is done in steps of 256 bytes (256 + 8 bits per memory circuit).
- The on-board memory is placed in the 4680 memory map in multiples of 2K segments.
- Address selection is done with an on-board jumper plug.
- Provides jumper selectable wait-state signalling.

The total access time is determined by the memory circuit chosen, the delays (3 TTL + bus) and CPU. If the access time does not match the concerned CPU then the memory module is adapted with the signal MEMRDY* , which requests for wait-states. For more information refer to System Manual and data sheets on the CPU-card.

The DataBoard requirements for 4680-bus signalling are contained.

SPECIFICATION

POWER	+ 5V ± 5 % – 12V ± 5 %
LOAD	+ 5V – 520 mA
SIZE	Standard Europe card 100 x 160 mm
CONNECTOR	64 pin standard Europe connector (DIN 41612)

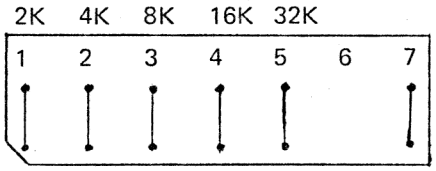
CONNECTION Any slot on the memory-side of the 4680-bus.

PIN NUMBERING See System Manual

SIGNALLING CPU 3003

- 16 bits addressbus
- 8 bits tristate databus
- MEMRDY* to be selected by the user for wait-state signalling.
- MEMFL* , the memory read signal

BASEADDRESS is selected on a jumper plug – on-board location 3C – as shown by the figure. The principle of coding is described in the System Manual.



Example:"1" and "3" cut results in (2 + 8 = 10) base address = 10 K. The module memory is allocated to 10 – 12K of the 4680 memory map.

MEMRDY* -signal is connected with the jumper B1. Jumper installed = wait-state signalling connected. The on-board location is shown by the figure.

ON-BOARD LOCATION OF MEMORY CIRCUITS

range	0-FF	100-1FF	200-2FF	300-3FF	400-4FF	500-5FF	600-6FF	700-7FF
position	1A	2A	3A	4A	1B	2B	3B	4B