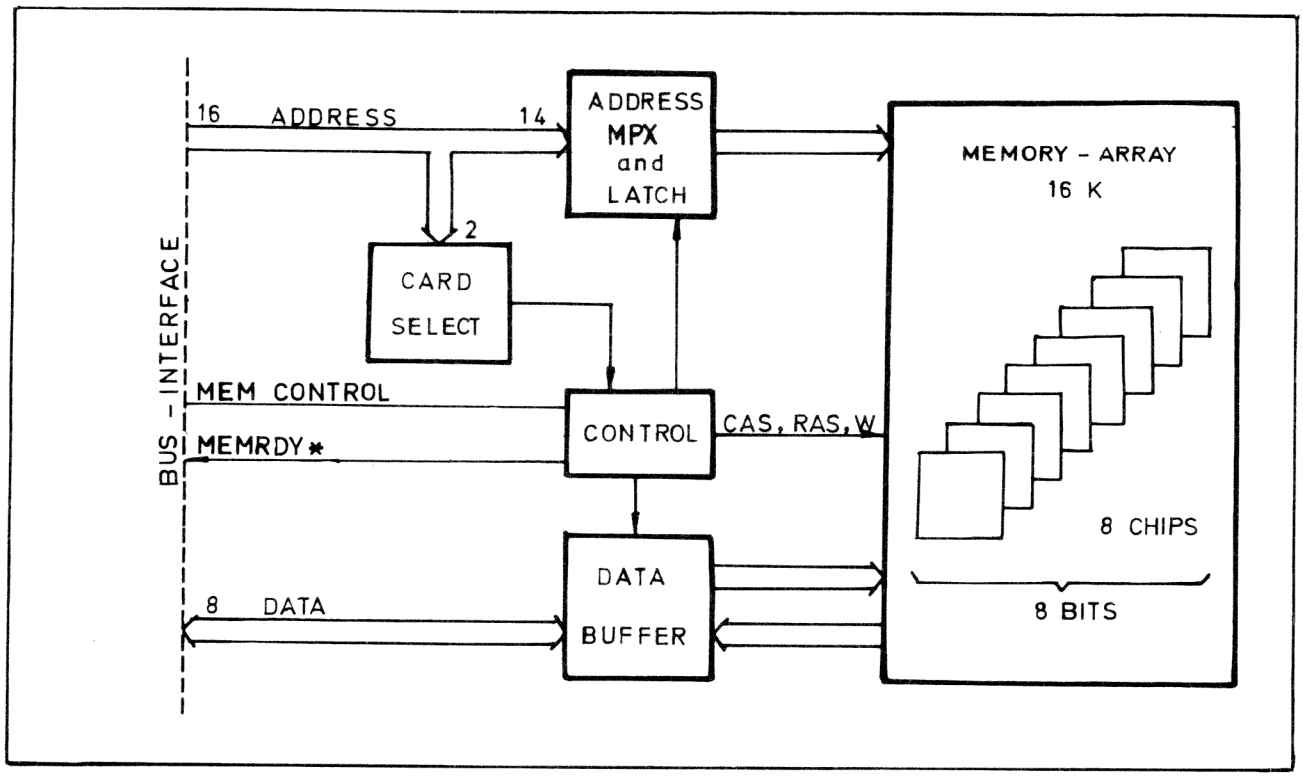


DESCRIPTION

2056 is a memory module for dynamic RAM based on memory circuit type 4116-3.

- It is delivered with full capacity 16 kbytes mounted.
- The on-board memory is placed in the 4680 memory map in multiples of 16K segments.
- Address selection is done by on-board switches.
- It is used in Z 80 double board applications. The double board computer provides refresh and cycle generetion.
- Facilitates DMA-use.

The total access time is determined by the memory circuit chosen, the delays (3TTL + bus) and CPU. The memory module is adapted to CPU with the signal MEMRDY* which requests for wait-state. For more information refer to the System Manual and data sheets on the concerned CPU-card.

The DataBoard requirements for 4680-bus signalling are contained.

SPECIFICATION

POWER	+5V±5%, 400mA +12V±5%, 40 mA -12V±5%, 20mA
ACCESS TIME	Nominal 200 ns exkl. system delays.
SIZE	Standard Europe card, 100 x 160 mm
CONNECTOR	B 64 pin standard Europe connector (DIN 41612)

CONNECTION — Any slot on the memory-side of the 4680-bus.

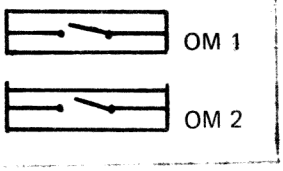
PIN NUMBERING — See System Manual

SIGNALLING CPU 2056

- 16 bits addressbus
- 8 bits tristate databus
- MEMRDY* is designed for requesting wait-stat
- MEM control comprises signals for read, write and refresh: MEMFL*, W*, ADMX*, RASST* CSTOP* and REFR*

Further information on bussignalling and conditions for wait-state can be studied in the System Manual.

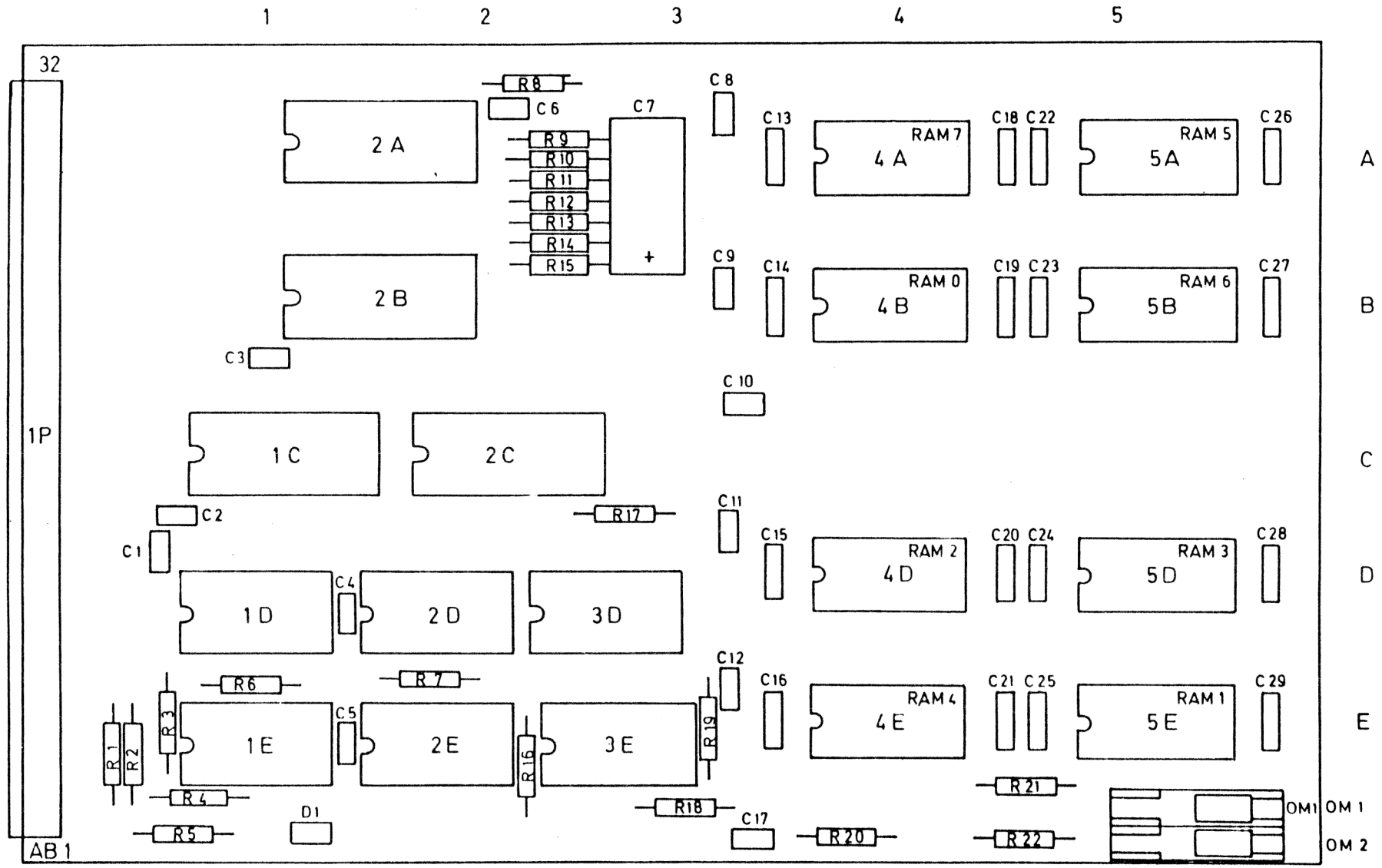
ADDRESS SELECTION — The Base Address of the module is selected with the switches OM1 and OM2 as tabled down. The onboard location is shown by the figure.



OM2	OM1	Memory area
ON	ON	0-16K
ON	OFF	16-32K
OFF	ON	32-48K
OFF	OFF	48-64K

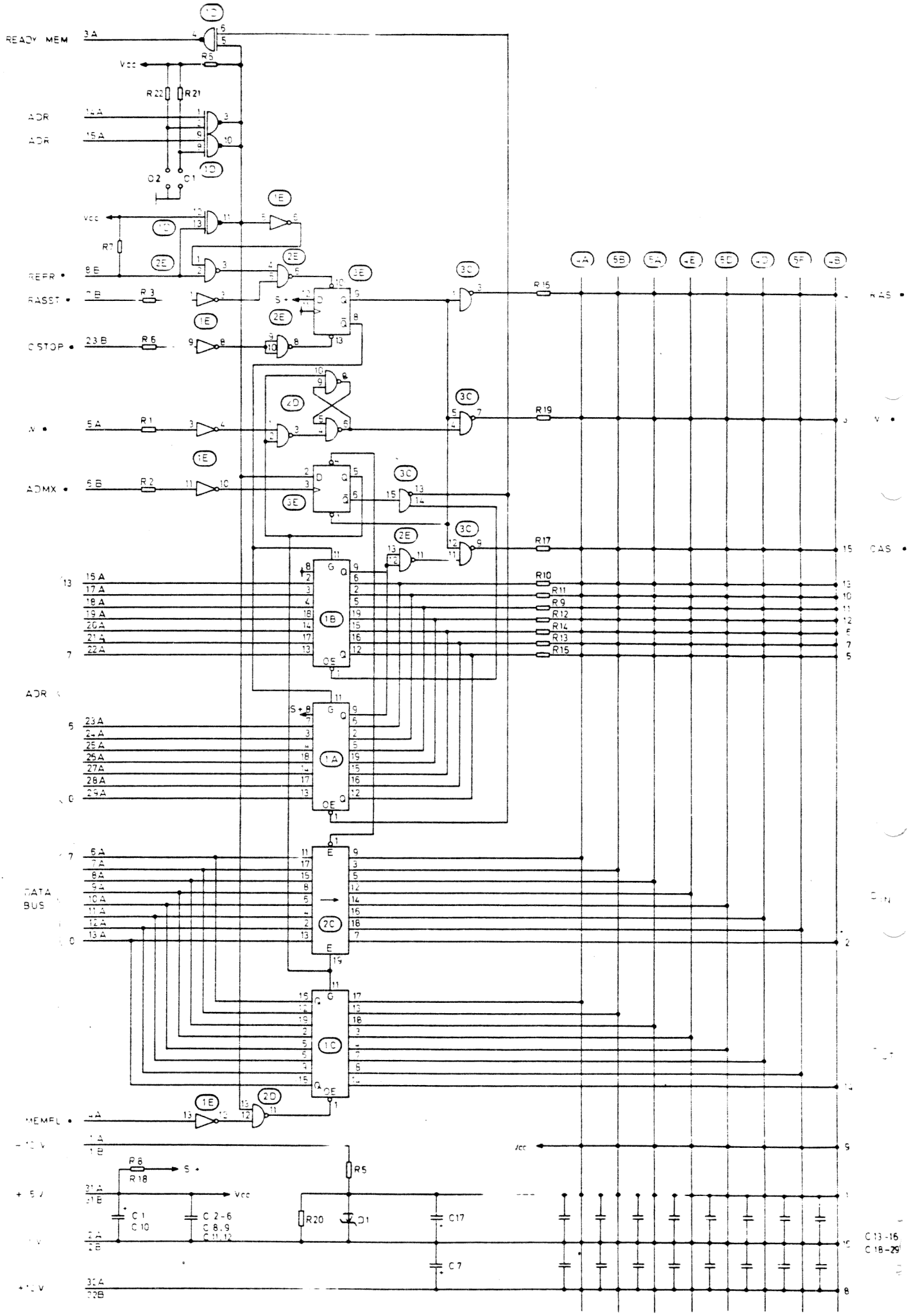
ON-BOARD LOCATION OF MEMORY CIRCUITS

	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Range 0-3FFF	4A	5B	5A	4E	5D	4D	5E	4B



NOTE RAM 0 CONTAINS THE LEAST SIGNIFICANT BIT (0) OF THE MODULE ARRAY.

		REV. NR	DATAINDUSTRIER AB	16 K RAM DYNAMIC	82-2056-00
		DATUM	TABY SWEDEN		



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DATAINDUSTRIER AB	
16 K RAM DYNAMIC	
81-2056-00	