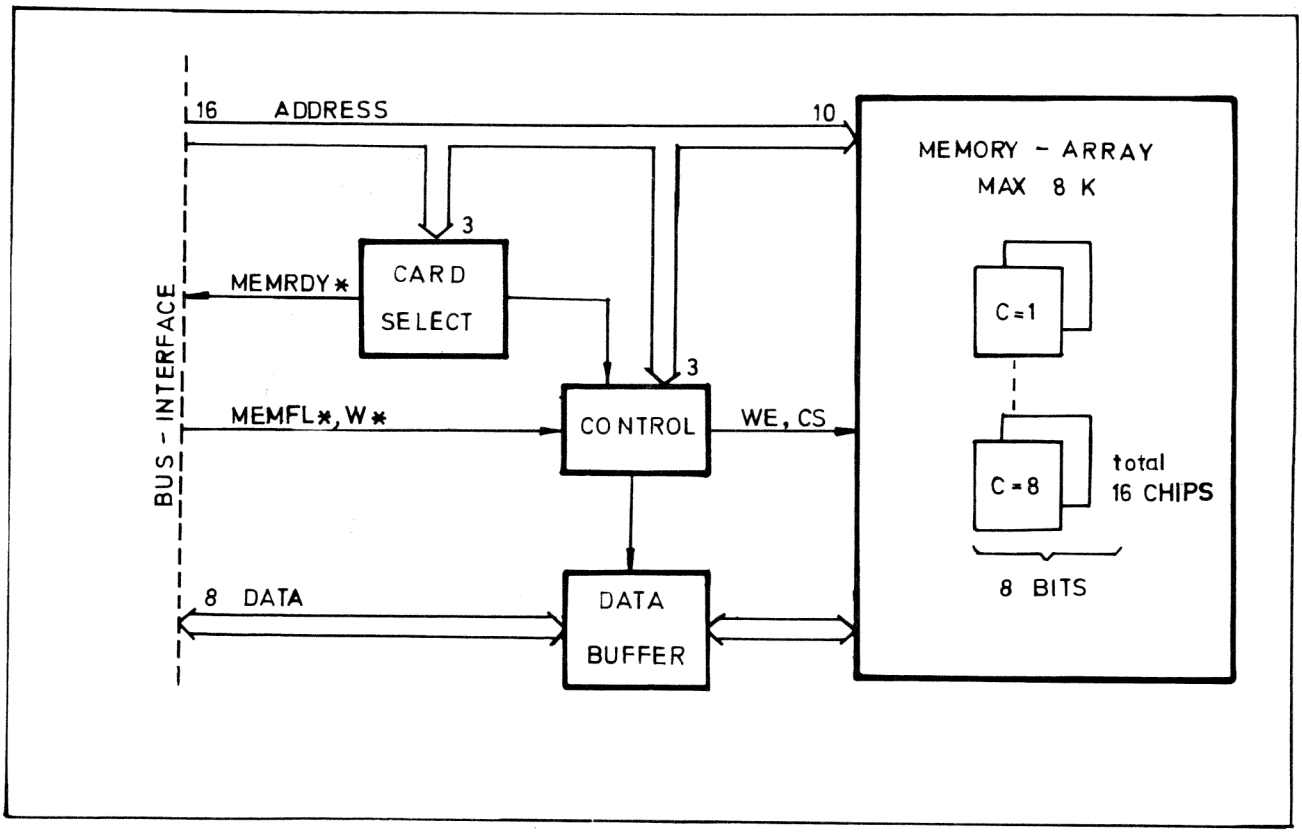
DATABOARD 4680

8K STATIC RAM

2055

JAN 82 1 2 x



DESCRIPTION

2055 is a memory module for static RAM based on memory circuit type SY 2114L-3 or equivalent.

- It is delivered with full capacity 8 K bytes mounted.
- The on-board memory is placed in the 4680 memory map in multiples of 8K segments.
- Address selection is done with an on-board jumper plug.
- Access time meets the requirements of DMA use.
- Provides jumper selectable wait-state signalling.

The total access time is determined by the memory circuit chosen, the delays (3 TTL + bus) and the CPU. If the access time does not match the concerned CPU then the memory module is adapted with the signal MEMRDY* which requests for wait-state (s). For more information refer to System Manual and data sheets on the CPU-card.

SATTCO AB DALVÄGEN 10 S-171 36 SOLNA SWEDEN PHONE 08/730 57 30 TLX 11588

SPECIFICATION

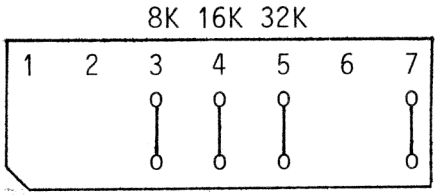
Power	+ 5 V ± 5 % max 1,2 A
Size	Standard Europe card 100 x 160 mm
Connector	B 64 pin two-row standard Europe connector (DIN 41612)
Connection	Any slot on the memory-side of the 4680-bus.
PIN NUMBERING	See System Manual

SIGNALLING CPU-2055

- 16 bits address bus
- 8 bits databus
- MEMRDY*
- MEMFL* and W* for memory read and write respectively.

JUMPERS — All optional functions are selected with the jumper-plug.

The module BASEADDRESS is selected on a jumper plug,on-board location 1D as shown by the figure. The principle of coding is described in the System Manual.



The MEMRDY* jumper installed = wait-state signalling connected.

Example: 3 and 4 cut gives (8 + 16 = 24K) memory segment 24 - 32K.

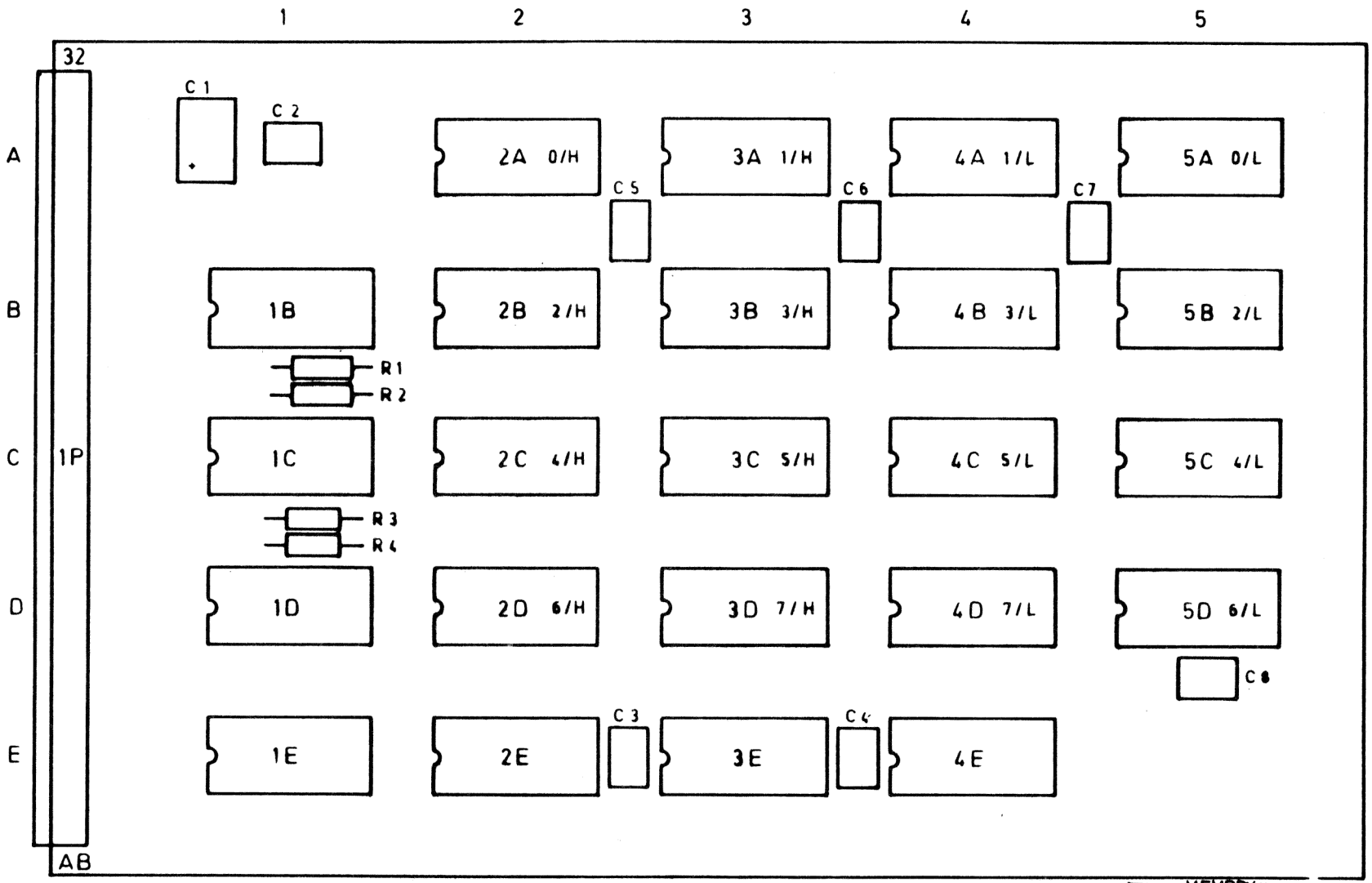
ON BOARD LOCATION OF MEMORY CIRCUITS

Range	0-3FF	400-7FF	800-BFF	C00-FFF	1000-13FF	1400-17FF	1800-1BFF	1C00-1FFF
bits 3 - 0 =	5A	4A	5B	4B	5C	4C	5D	4D
bits 7 - 4 =	2A	3A	2B	3B	2C	3C	2D	3D

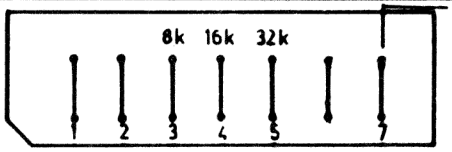
ACCESS TIME DELAYS

The 2055 delays in access time calculations are on the bus connector:

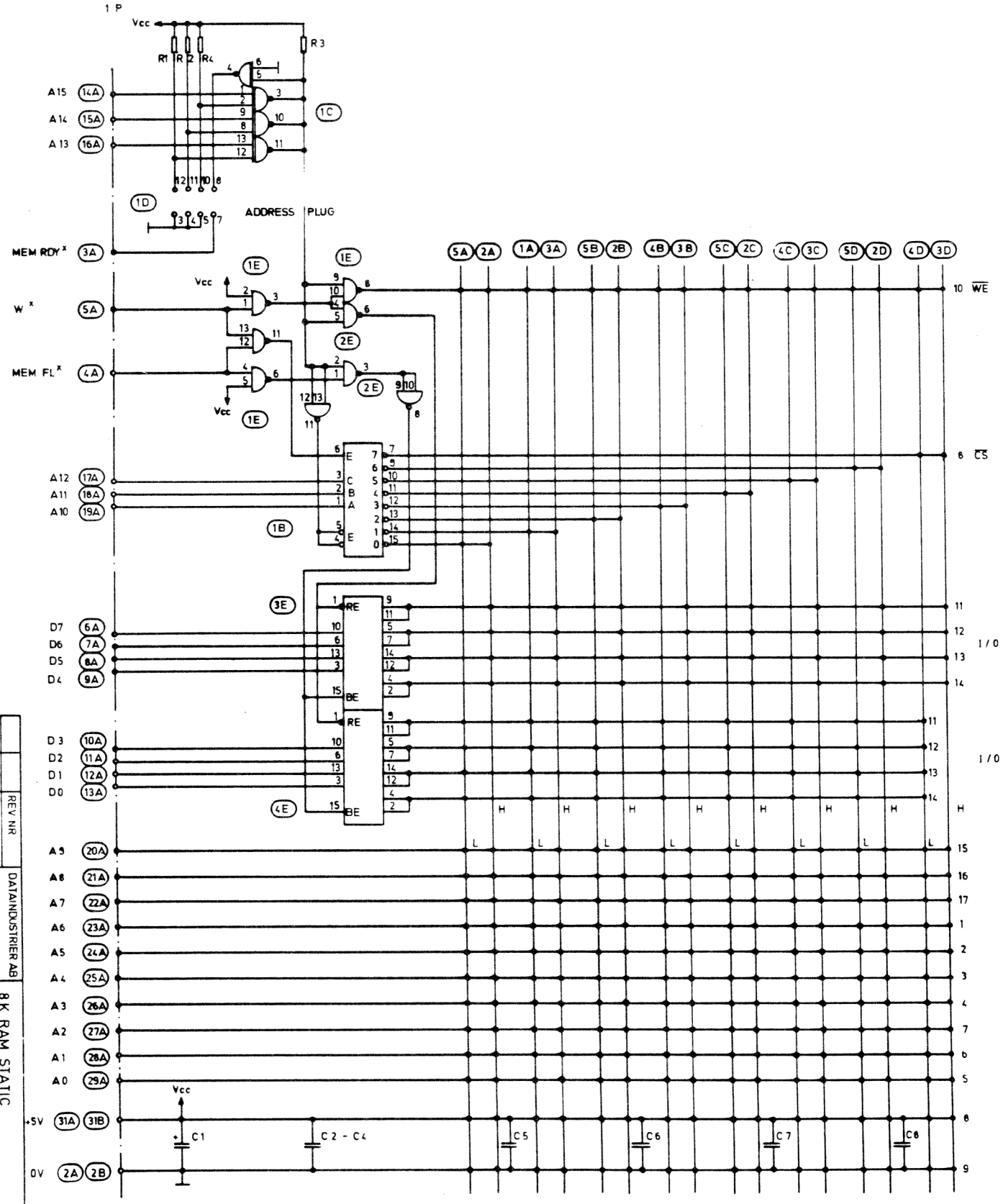
From ADDRESS to DATA		17 nsec + Tacc
	or	94 nsec + Tce
From MEMFL* to DATA		77 nsec + Tce



NOTE MEMORY ADDRESS IS SPECIFIED FOR EACH MEMORY CIRCUIT. THE FIRST 1k ARRAY IS PLACED IN 2A FOR HIGH ORDER BITS (7-4) AND 3A FOR LOW ORDER BITS (3-0).



	A	REV NR	DATAINDUSTRIER AB	8 K RAM STATIC	82-2055-00
	79.03	DATUM	TÄBY SWEDEN		


1 P
Vcc
R1 R2 R4
R3
A15 14A
A14 15A
A13 16A
1C
1D
ADDRESS PLUG
MEM RDY X 3A
W X 5A
MEM FL X 4A
1E
2E
A12 17A
A11 18A
A10 19A
1B
3E
4E
D7 6A
D6 7A
D5 8A
D4 9A
D3 10A
D2 11A
D1 12A
D0 13A
A9 20A
A8 21A
A7 22A
A6 23A
A5 24A
A4 25A
A3 26A
A2 27A
A1 28A
A0 29A
+5V 31A 31B
0V 2A 2B
C1
C2 - C4
C5
C6
C7
C8
5A 2A
1A 3A
5B 2B
4B 3B
5C 2C
4C 3C
5D 2D
4D 3D
10 WE
6 CS
I/O
I/O
H
L