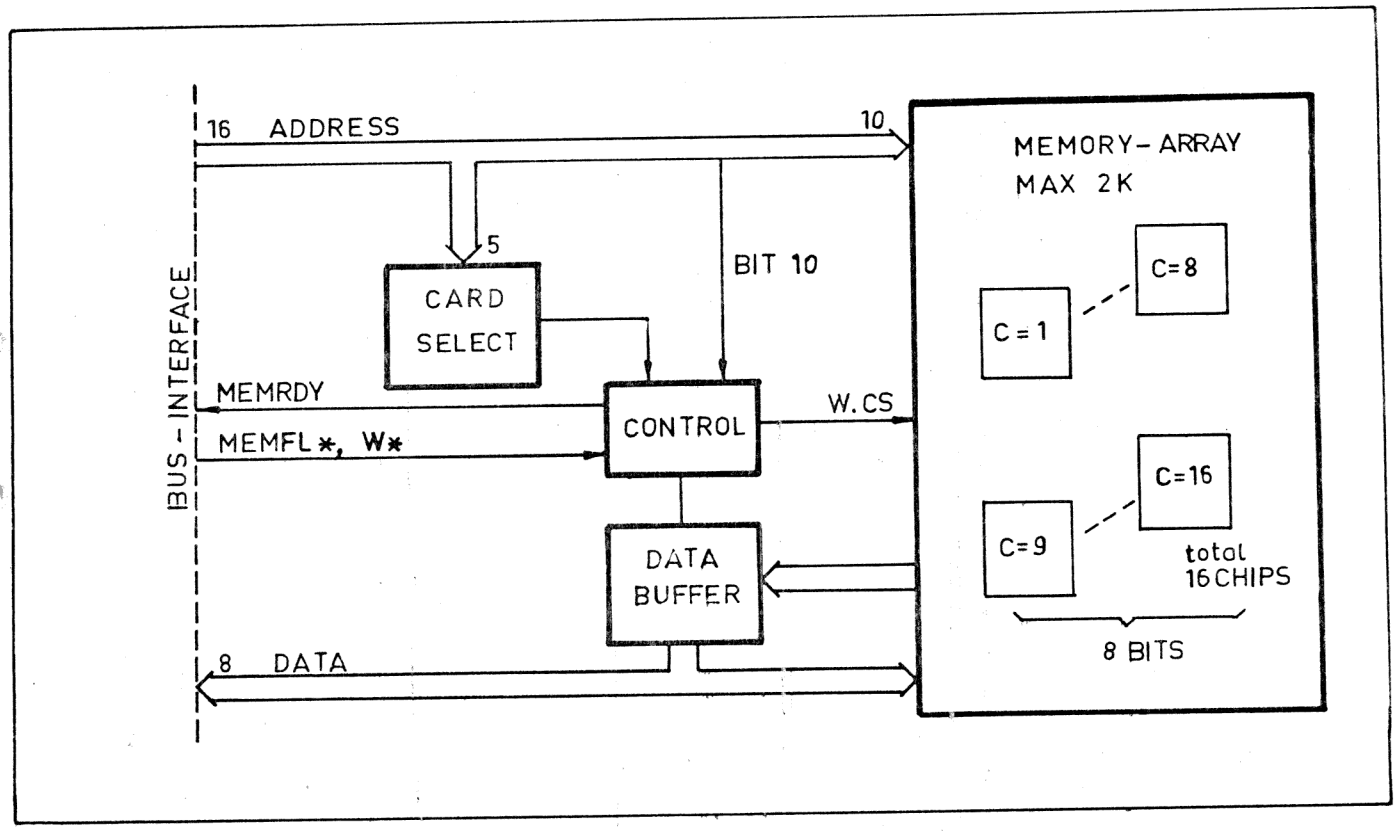
Jan 79



DESCRIPTION

2002 is a memory module for static RAM based on memory circuit 21L02B

- It is delivered with full capacity of 2 kbytes mounted.
- The on-board memory is placed in the 4680 memory map in multiples of 2K segments.
- Address selection is done with an on-board jumper plug.
- Memory circuits are inserted in steps of 1K (8 memory circuits).
- Provides jumper selectable wait-state signalling.

The total access time of the memory module in a system is determined by the memory circuit chosen and the delays (3TTL + bus). If the access time does not match the concerned CPU then the memory module is adapted with the signal MEMRDY* , which requests for wait-state(s). For more information refer to the System Manual and data sheets on the CPU-card.

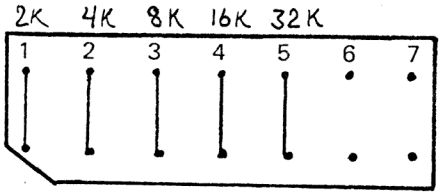
The DataBoard requirements for 4680-bus signalling are contained.

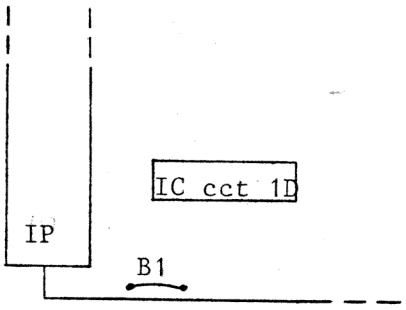
SPECIFICATIONS

	POWER	+ 5V ± 5% 480 mA
	SIZE	Standard Europe card 100 x 160 mm
	CONNECTOR	64 pin two-row standard Europe connector (DIN 41612)
CONNECTION		Any slot on the memory-side of the 4680-bus.
PIN NUMBERING		See System Manual
SIGNALLING CPU-2002		– 16 bits addressbus – 8 bits tristate databus – MEMRDY* to be selected by the user for wait-state signalling – MEMFL* , the memory read signal

JUMPERS

BASEADDRESS is selected by a jumper plug-on-board location 1B - as shown by the figure. The principle of coding is described in the System Manual.





The MEMRDY* -signal is connected to the bus-connector by jumper B1 located directly beneath the IC-circuit 1D.

ON-BOARD LOCATION OF MEMORY CIRCUITS

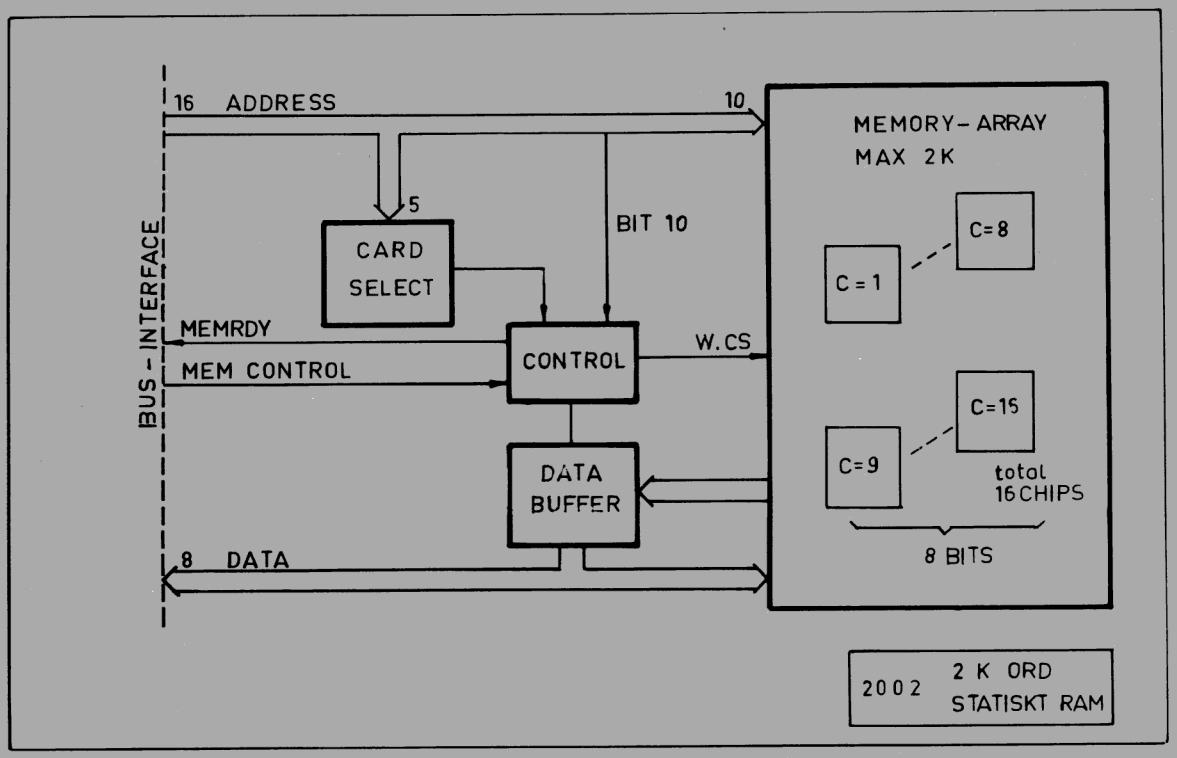
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Range 0–1K =	3B	4B	5B	6B	3A	4A	5A	6A
Range 1–2K =	3D	4D	5D	6D	3C	4C	5C	6C

DATABOARD 4680

2K ORD STATISKT RAM

2002

April 1978



BESKRIVNING

2002 är ett statiskt RAM som baserats på minneskrets 21LO2B.

- **Det är vid leverans fullt bestyckat med 2 kbyte (1024 x 1 bitar per kapsel)**
- **Det kan läggas valfritt inom 64K med multipel av 2K.**

  Adressval sker med bygglingsplugg.
- **Det kan bestyckas i steg av 1 kbyte.**

  Kortet uppfyller buss–normerna för last– och drivförmåga i

  DataBoard 4680.

SATTCO AB · DALVÄGEN 10 · 171 36 SOLNA · TFN 08/83 02 80

TEKNISKA DATA:

– Matningsspänning:	5V ± 5%
– Strömförbrukning fullt bestyckad:	480 mA
– Accesstid:	Nominellt 400 nsek för typ 21LO2B
– Mått:	Enkelt europakort 100 x 160 mm
– Kontakt:	B 64 pol. tvåradigt europadon 41612

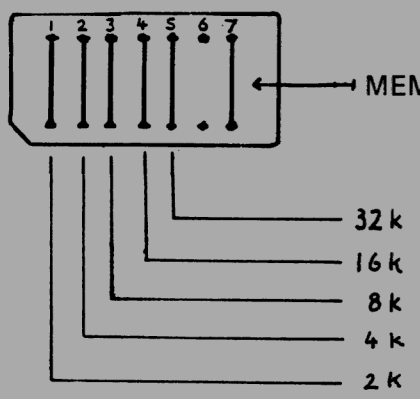
KONTAKTNUMRERING: Se systembeskrivning

SIGNALER mellan CPU och RAM–kort:

- 16 bitars adressbuss
- 8 bitars tristate databuss
- MEMRDY är konstruerad för att begära två "wait–states" av CPU
- "MEM control" innehåller signalerna för läsning, MEMFL och skrivning

Anm. Systembeskrivningen beskriver bussignalerna och anger villkoren för MEMRDY.

Byglingar: Minnets placering i minnesarean väljs med byglingsplugg.



Exempel: 1 och 3 klippta ger
(2+8=10) minnesarean 10 – 12K