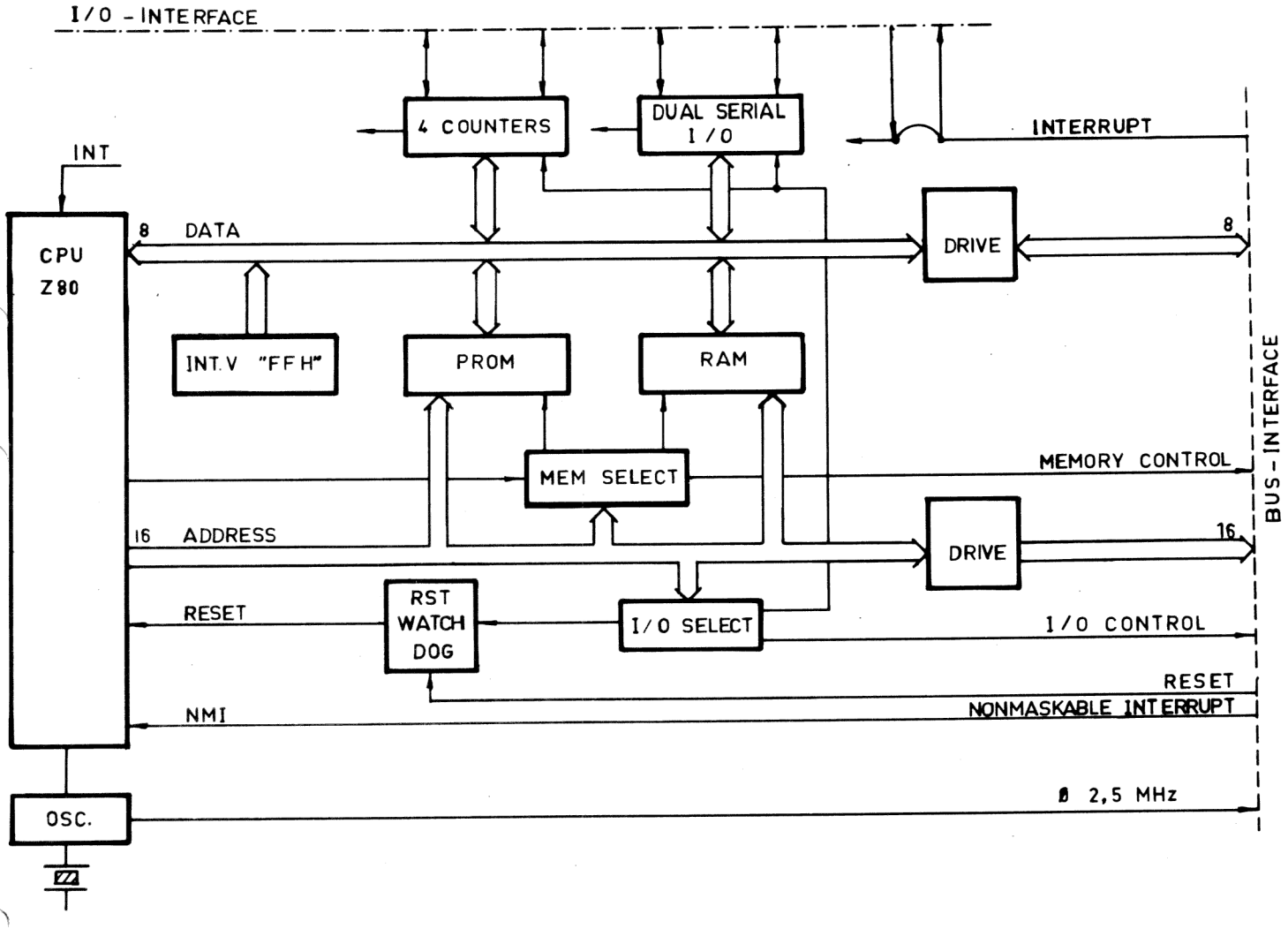
DATABOARD 4680

Z 80 – SIO
SINGLE BOARD COMPUTER

1062

PRELIMINARY

AUG 80 | 1 | 5



DESCRIPTION

1062 is a single board computer based on Z 80 CPU, CTC and SIO. It provides interfacing to the 4680 - bus and two channels of data communication.
1062 is designed to be used in small applications with the required memory on-board. Memory - and I/O - expansion is done through the 4680 - bus.

By using option SIO-Booster 5098, the two channels of data communications may be interfaced to standard V24.

The single board computer does not include use of dynamic RAM and DMA. The double board computer 1043/1044 and a special interface card for data communication is chosen in these cases and when more than 2 interrupt levels are required.

SATTCO AB, DALVÄGEN 10, 171 36 SOLNA, TEL. 08-730 57 30, TLX 11588

SPECIFICATION

NUMBER OF INSTRUCTIONS		158, includes 4, 8 and 16-bits operations.
CYCLE TIME		1,6 / us for register to register operations.
MEMORY	**PROM**	2 sockets for any of the types 2708, 2716, 2732 or 2758. The on-board capacities of 2, 4, 8 and 2 kbytes respectively are provided.
	RAM	1 kbytes static RAM, type 2114.
MEMORY ADDRESSING		On-board PROM, see "options" RAM, FCOOH – FFFH
MEMORY EXPANSION		Up to 64 kbytes of RAM:s and (E)(P)ROM:s in any combination through the 4680 - bus. Use standard modules from DataBoard 4680.
I/O- CAPACITY		2 channels for data communication. Counters (clocks), 4 trigger inputs and 3 outputs.
INTERRUPTS		2 levels: NMI, nonmaskable interrupt INT, common level for I/O
PROGRAM CONTROL		Through watch - dog.
REAL TIME CLOCK		Provided through on-board counter on system or external clock.
SYSTEM CLOCK		2,5 MHz crystal controlled.
INTERFACING		Both the I/O- and businterfaces are TTL-compatible. All bussignals are buffered. The outputs may be connected to standard V24 if SIO-Booster 5098 is used.
POWER		+ 5V± 5%, 1,4A excluding (P)ROM If 2708 PROM then also "-5V option" including: + 12V ± 5% – 12V ±5%
CONNECTOR		64-pin two-row Europe connector (DIN 41612) on both I/O- and bus-sides.
ENVIRONMENT		Operating O – + 55° C.

THE SERIAL INTERFACE

Two channels provide serial asynchronous or synchronous data transfer. CRC is available. The channels are programmed I/O- ports and hence very flexible. All traditional asynchronous communications are managed.

I/O CONTROL

Is standard DataBoard 4680 I/O-bus signalling. See System Manual. It comprises control of watch-dog and I/O-reset. Internal on-board I/O, the serial communication and the counters are not included in normal 4680 I/O - commanding. These are operated in correspondence with the product specifications of the Z 80 - CTC and -SIO. Running operations on the I/O-bus can be multiplexed with the on-board I/O without disturbances from each other. The channel selection of the I/O-bus stands unchanged.
Internal I/O addresses are as follows:

Counter	0	1	2	3
Address	30H	31H	32H	33H

Channel	A-data	A-control	B-data	B-control
Address	38H	39H	3AH	3BH

INTERRUPT

The interrupt handling is connected to and completely controlled by the internal I/O. It comprises the nonmaskable interrupt (NMI) from the bus and a maskable interrupt INT. The latter is common for the whole I/O.
NMI has the vector 66H.

INT is mode-controlled by the programmer.

The vector in mode O and 2 are determined by the loaded values in CTC and SIO. If none of these responds to the signal the vector FFH is sent to the CPU. On-board jumper facilitates for alternative interrupts. The interrupt may be connected for the I/O-bus signalling solely. It can be connected via I/O-connector and any of the available internal ports. These two alternatives may be combined.

The input of counter O has the highest priority (next to NMI) and channel B (mode 3) the lowest priority.

The NMI can be used for actions needing fastest response as for example "Power-down".

RESTART

This function is available through internal "program control by hardware" (watch-dog). Restart resets CPU and initiates program run on address O. The function is also activated by "power - on". Manual restart and disconnection of the watch-dog is available via the bus. The input and output functions are reset at "power-on" and by a specific out-command.

MEMORY CONTROL

The single board computer provides memory expansion through the 4680-bus interface which contains memory control as follows:

MEMFL — for memory read
W — for memory write
and 16 bits address.

When selecting memory the user must consider the maximum total access times given below. The total access time is calculated to the access time of the memory circuit on the module plus standard 100 nsec . for delays (3TTL, bus and CPU).
The maximum total access times allowed are:

1) 550 nsec - for instruction fetch
2) 750 nsec - for access of data
3) 750 nsec - for input/output operations

4680 - BUS INTERFACING

Standard and flexible expansion is provided through ready to use backplanes. 8, 14 and 20 slot backplanes are available. The user has also the choice of managing the backplanes wiring himself. Bus-wiring and signals are presented in the System Manual.

The single board computer may use the backplanes of the double board computer by plugging the 1062 into the Control Unit slot and a jumper board into the CPU slot. See System Manual. The 8-slot backplane is designed single board computers only.

PIN NUMBERING - INTERNAL I/O

Pin	29A	Interrupt out	See "options"
	25A	Interrupt in	

The signal names are the same as used in the prod. spec.:s of Z 80 - CTC resp. SIO.

COUNTERS (CTC)

Signal	0 IN	0 OUT	1 IN	1 OUT	2 IN	2 OUT	3 IN
Pin	5B	6B	6A	7B	7A	8B	8A

SERIAL COMMUNICATION

Channel A

Signal	RXD	$\overline{\text{RXC}}$	$\overline{\text{TXC}}$	TXD	$\overline{\text{SYNC}}$	$\overline{\text{RTS}}$	$\overline{\text{CTS}}$	$\overline{\text{DTR}}$	$\overline{\text{DCD}}$
Pin	13B	27B	25B	12B	19B	14B	15B	30B	18B
Modem	3	17	15	2	9	4	5	2	8

Channel B

Signal	$\overline{\text{DCD}}$	$\overline{\text{DTR}}$	$\overline{\text{CTS}}$	$\overline{\text{RTS}}$	RXD	TXD	$\overline{\text{TXC}}$	$\overline{\text{RXC}}$
Pin	22B	28B	23B	29B	20B	24B	21B	26B
Modem	12	18	13	19	10	14	11	16

0-volt pin	2A-B
+ 5V	31A-B
+ 12V	32A-B

JUMPERS

Selection of PROM-type and memory segment for on-board memory.

2708	b1c	b2c	b3(inserted)	and	b4(inserted)	0-7FFH
2716	b1b	b2b	b3(open)	and	b4(inserted)	0-FFFH
2732	b1b	b2a	b3(inserted)	and	b4(open)	0-1FFFH
2758	b1a	b2b	b3(inserted)	and	b4(inserted)	0-7FFH
no on-board memory			b3(open)	and	b4(open)	-

The card is delivered with the bus initiated interrupt connected to the maskable interrupt (INT),jumper b5.

Next page shows where the jumpers are located.

OPTION

The – 5V option for using 2708 requires following components:

/uA 79 MO5AHC

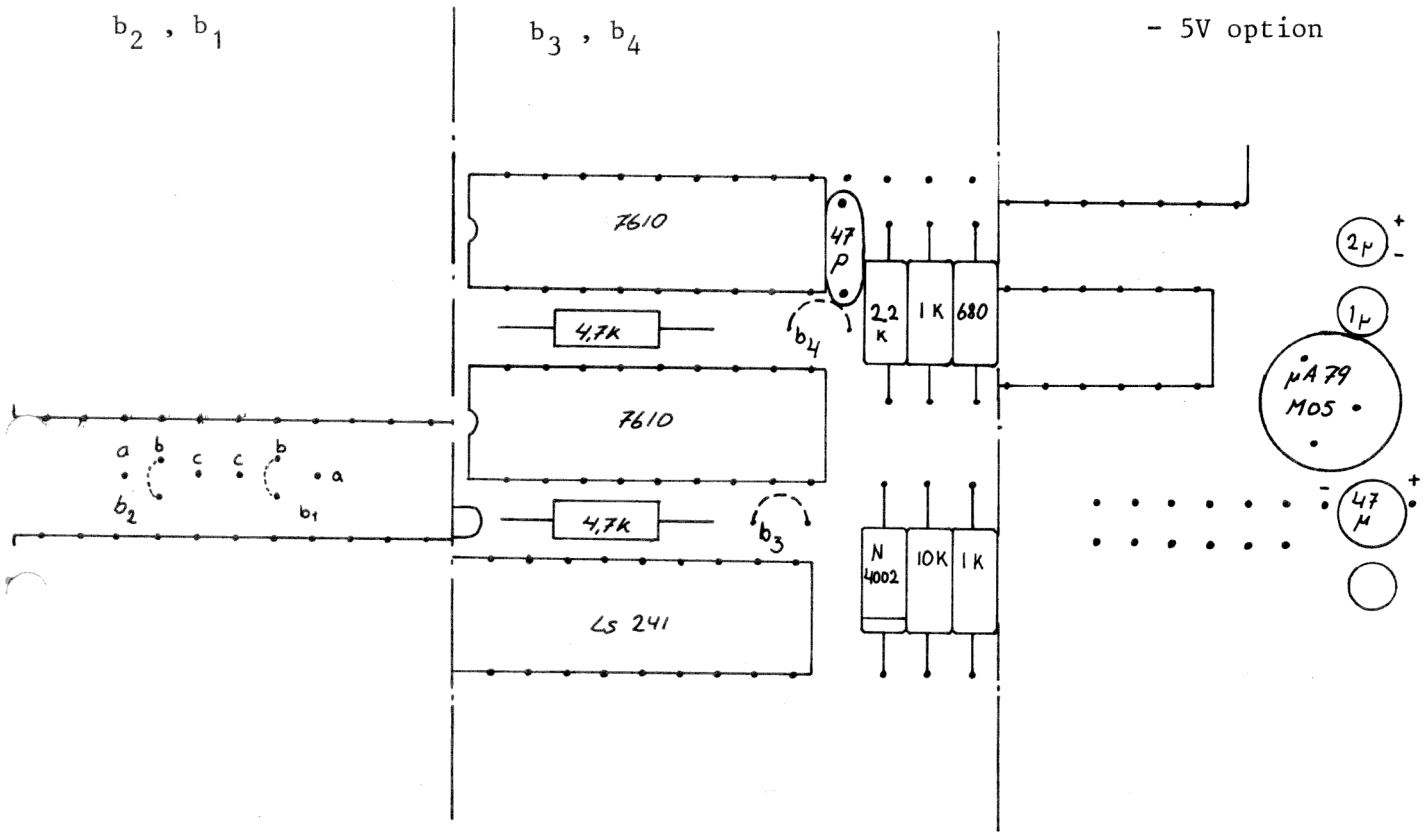
cond., tantal, drop	1 /uF 16V
codn., tantal, drop	2 /uF 16V

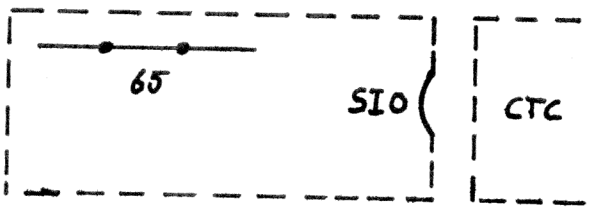
Figure on the next page shows where the components are to be placed.

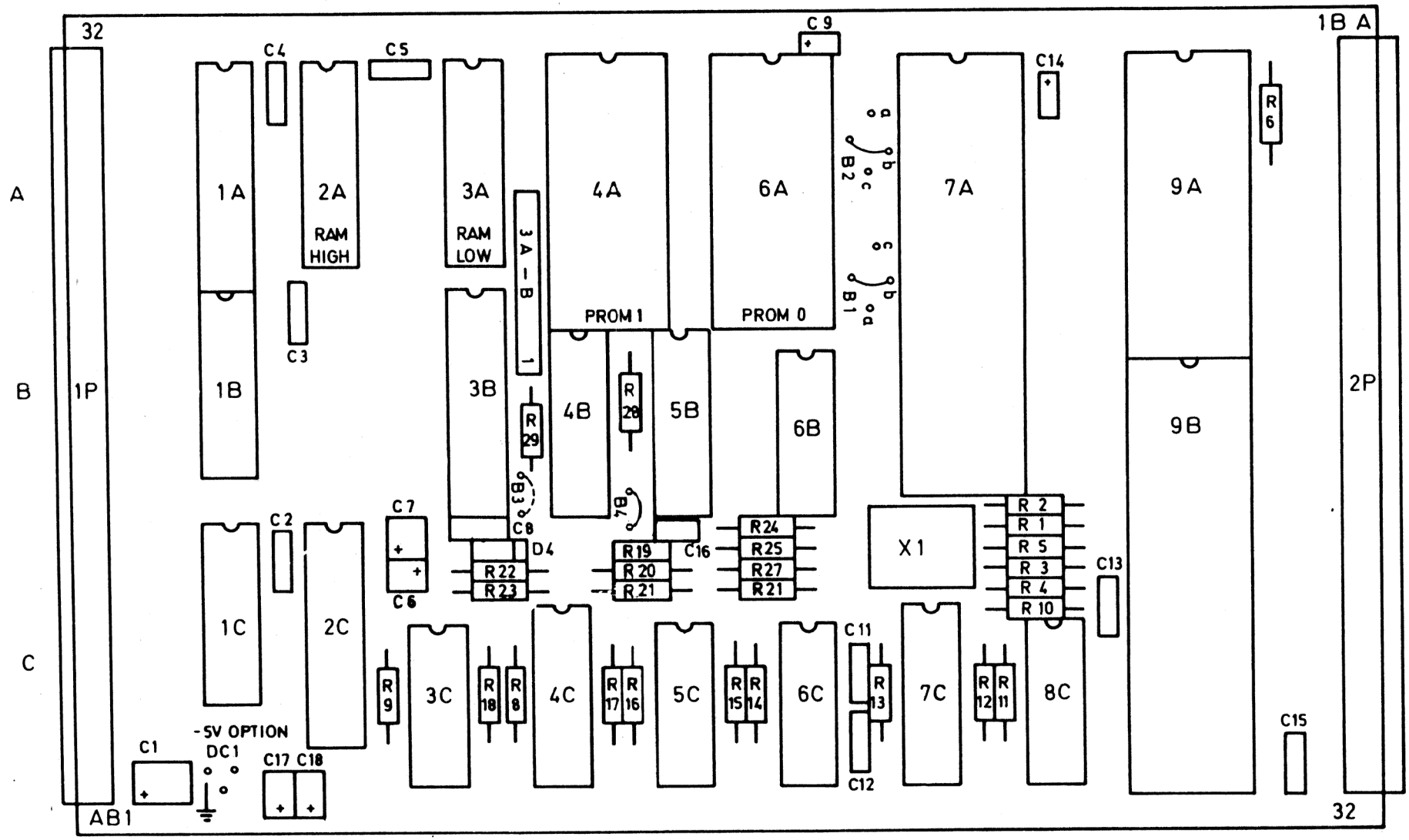
Ref.

The System Manual presents the DataBoard concept and provides details on system functions, bussignalling etc.

ON-BOARD LOCATION OF JUMPERS AND OPTIONS







COMMENT: SELECT TYPE OF MEMORY BY JUMPERS B1 - B4.
THE JUMPER AND JUMPER ALTERNATIVES NOT MENTIONED ARE ASSUMED OPEN.

-2758 ; INSTALL B1/a, B2/b, B3 AND B4.
-2708 ; INSTALL B1/c, B2/c, B3 AND B4.
-2716 ; INSTALL B1/b, B2/b AND B4.
-2732 ; INSTALL B1/b, B2/a AND B3.

PROM 0 SIGNIFIES THE LOW ADDRESS INTERNAL PROM MEMORY.
RAM LOW RESP. HIGH ARE THE LOW (3-0) AND HIGH (7-4) ORDER BITS OF THE INTERNAL 1k RAM.

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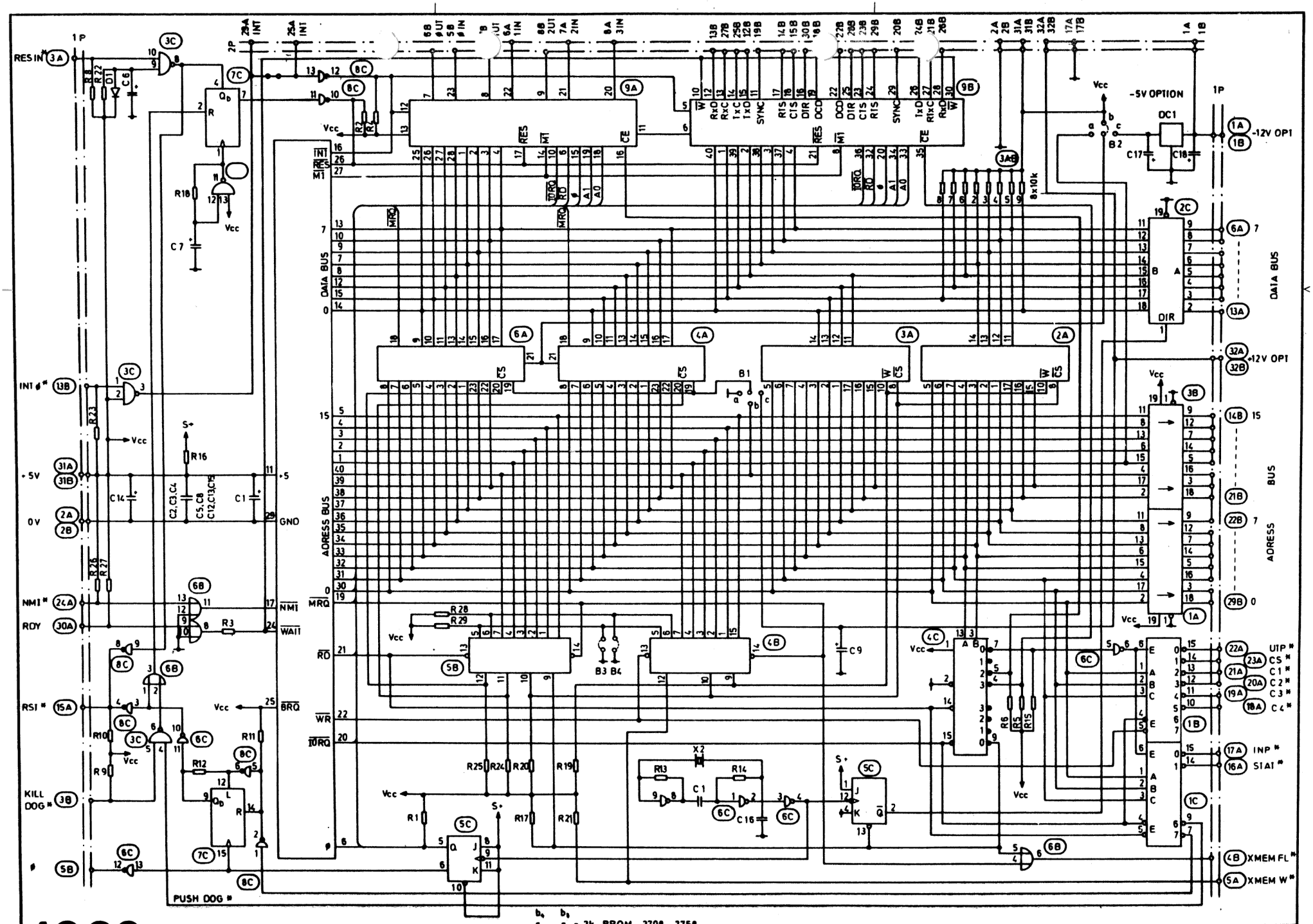
1062
ENKORTSDATOR SIO
4680 B62
DATAINDUSTRIER AB
TÄBY SWEDEN
REV NR
DATUM
DATA BUS
ADRESS BUS
-5V OPTION
-12V OPT
+12V OPT
RESIN
INT
NMI
RDY
WAIT
RSI
KILL DOG
PUSH DOG
XMEM FL
XMEM W
INP
STAI
UTP
CS
C1
C2
C3
C4
b1a 2758
b1b 2716, 2732
b1c 2708
b2a 2732
b2b 2758, 2716
b2c 2708
b0 b1
s = 2k PROM 2708, 2758
s = 4k " 2716
s = 8k " 2732
s = no internal memory