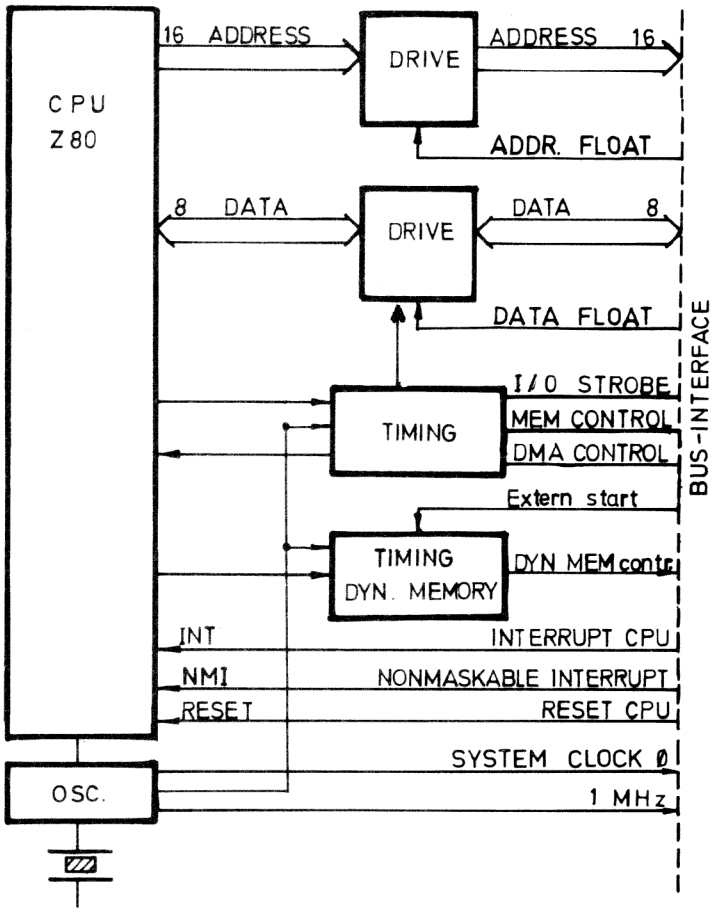


DESCRIPTION

1043 is the CPU-board of the Z 80 double board computer. The Control Unit 1044 is the other part.

1043/1044 provides full availability of the 4680-bus and the standard mudules in the range of DataBoard 4680. DMA and dynamic RAM on the memory-side of the bus can be used. Expanded levelled interrupt handling is provided. Restart combined with hardware-control of program flow is implemented. Optional on-board PROM provides program load at restart. I/O-trace is available as an option.

1043 comprises CPU, oscillator and drivers for the bus connection. It provides cycle generation for the dynamic memories and logic to synchronize slow memories and I/O.

I/O and the system functions for restart and I/O-trace are implemented in 1044.

SPECIFICATION

NUMBER OF INSTRUCTIONS	= 158, includes 4,8 and 16 bit operations
CYCLE TIME	1,6 µs for register to register operation at standard system clock.
MEMORY	Expandable up to 64 kbytes through the 4680-bus. Standard modules of RAM:s and (P) ROM:s provided in DataBoard 4680.
I/O	See 1044
INTERRUPT	NMI (nonmaskable interrupt) INT (maskable interrupt), see 1044.
SYSTEM CLOCK	Standard 2,5 MHz.
INTERFACING	Busdrivers and busreceivers.
POWER SUPPLY	+5V ± 5% 490 mA
CONNECTORS	64 pin double row standard Europe (DIN 41612) connector.
SIZE	Standard Europe card, 100 x 160 mm.
ENVIRONMENT	Operating 0 - + 55°C.

4680-BUS INTERFACING

Standard and flexible expansion is provided through ready to use backplanes. 14 and 20 slot racks are available.

The double board computer is plugged into the backplane in fixed places with the 1043 on the memory-side and 1044 on the I/O-side.

MEMORY CONTROL

All types of memory-modules contained in the DataBoard 4680 concept are available. 1043 facilitates cycle generation and refresh for dynamic memories. Slow units, connected to the CPU, are synchronized through wait-state-signalling. The concerned unit requests wait-state(s) by the MEMRDY(*)-signal.

The conditions for wait-state(s) are stated as follows:

1) "Instruction fetch" requires wait-state(s) if the access-time is longer than 550 ns.

2) "Memory-access" for data requires wait-state(s) if the access-time is longer than 750 ns.

3) Input/Output-operations require wait-state(s) if the access-time is longer than 750 ns.

Note. The values refer to the total access-time comprising memory circuit and system delays.

Following bussignals initiate wait-state(s):

- READY(*), unlimited wait
- IORDY(*), maximum 2 wait-states at I/O-operations.
- MEMRDY(*), maximum 2 wait-states at memory access.

Note. The presented time values assume standard system clock. One wait-state is 400 ns.

1 wait-state for dynamic RAM-modules

2 wait-states for static RAM-, PROM- and I/O-modules.

INTERRUPT HANDLING

1 nonmaskable and 8 masked levels of interrupt priorities are provided. The interrupt MODE, which the programmer chooses, determines vectors as follows:

MODE 0 (8080A)	The interrupt is provided by 1044 as an RST-instruction. See 1044.
MODE 1	CPU will respond to an interrupt by executing a restart to location 0038H.
MODE 2	The vectors are delivered by the 1044, which determines the 8 least significant bits. The sector address is determined by the 8 most significant bits in the programloaded I-register. The Z 80-CPU will combine the I-register contents with the interrupt acknowledge vector to form a 16-bit address which accesses the interrupt address vector table created by programmer. Z 80-CPU will execute a call to the memory location obtained from interrupt address vector table.

The nonmaskable interrupt (NMI) initiates a subroutine call to address 0066H.

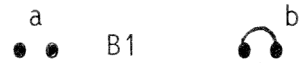
SPECIAL FUNCTIONS

1 MHz clock is delivered to the bus.

JUMPERS

Jumpers for wait-state(s) at memory access shall be inserted as follows, one of the available jumpers must be chosen.

"WAIT on ALL MREQ"
Results in wait-state(s) at
all memory accesses.



on-board location 2A-B

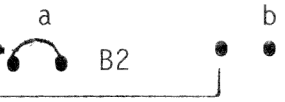
"WAIT ON M1-MREQ"
Results in wait-state(s) at
"instruction fetch" only.

The card is delivered with
this jumper installed.

B1/b installed at shipping

Jumpers for the bus-signal Ø-USRT

Ø buffered
Ø/2, nonbuffered



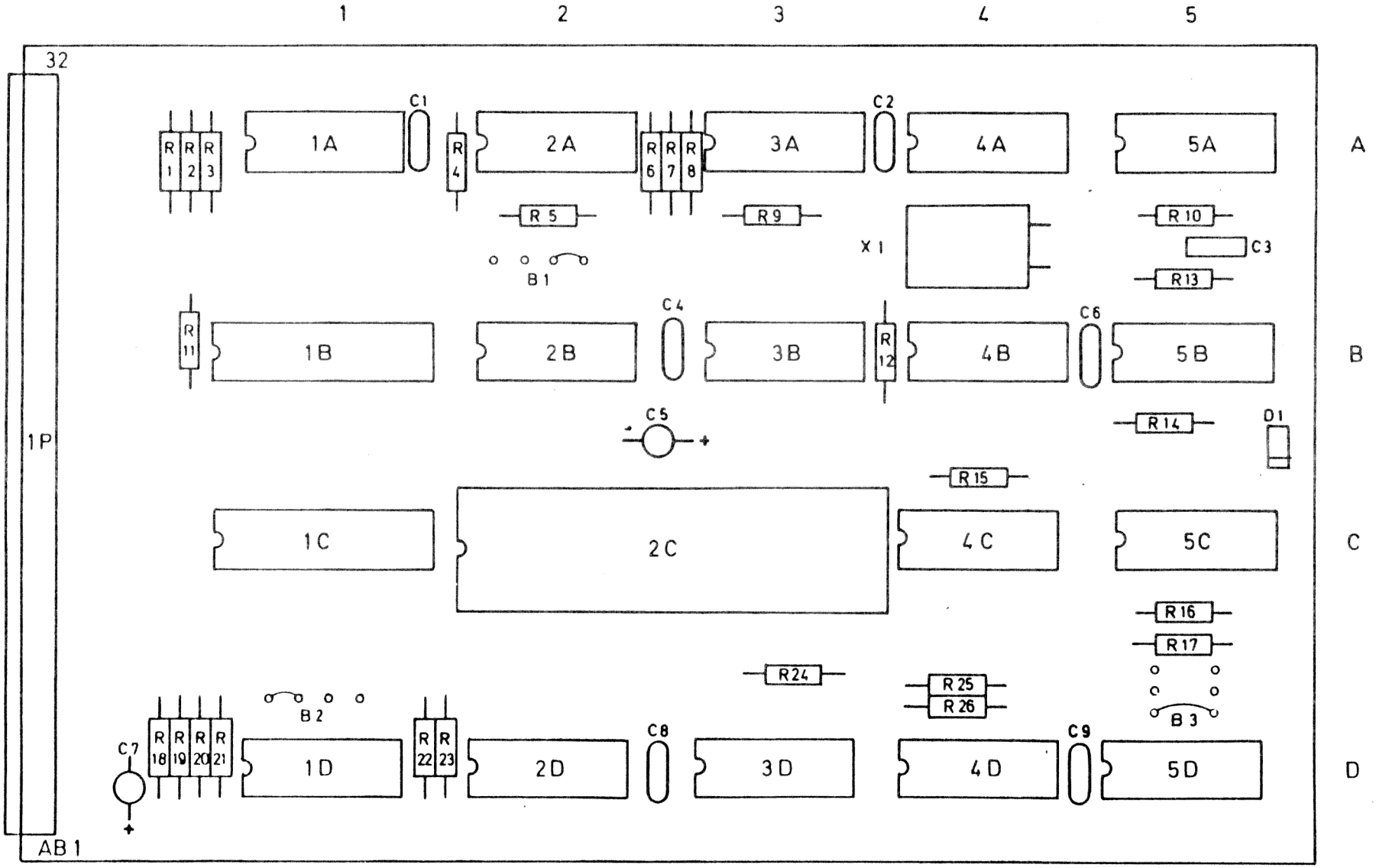
on-board location 1C-D

B2/a installed at shipping

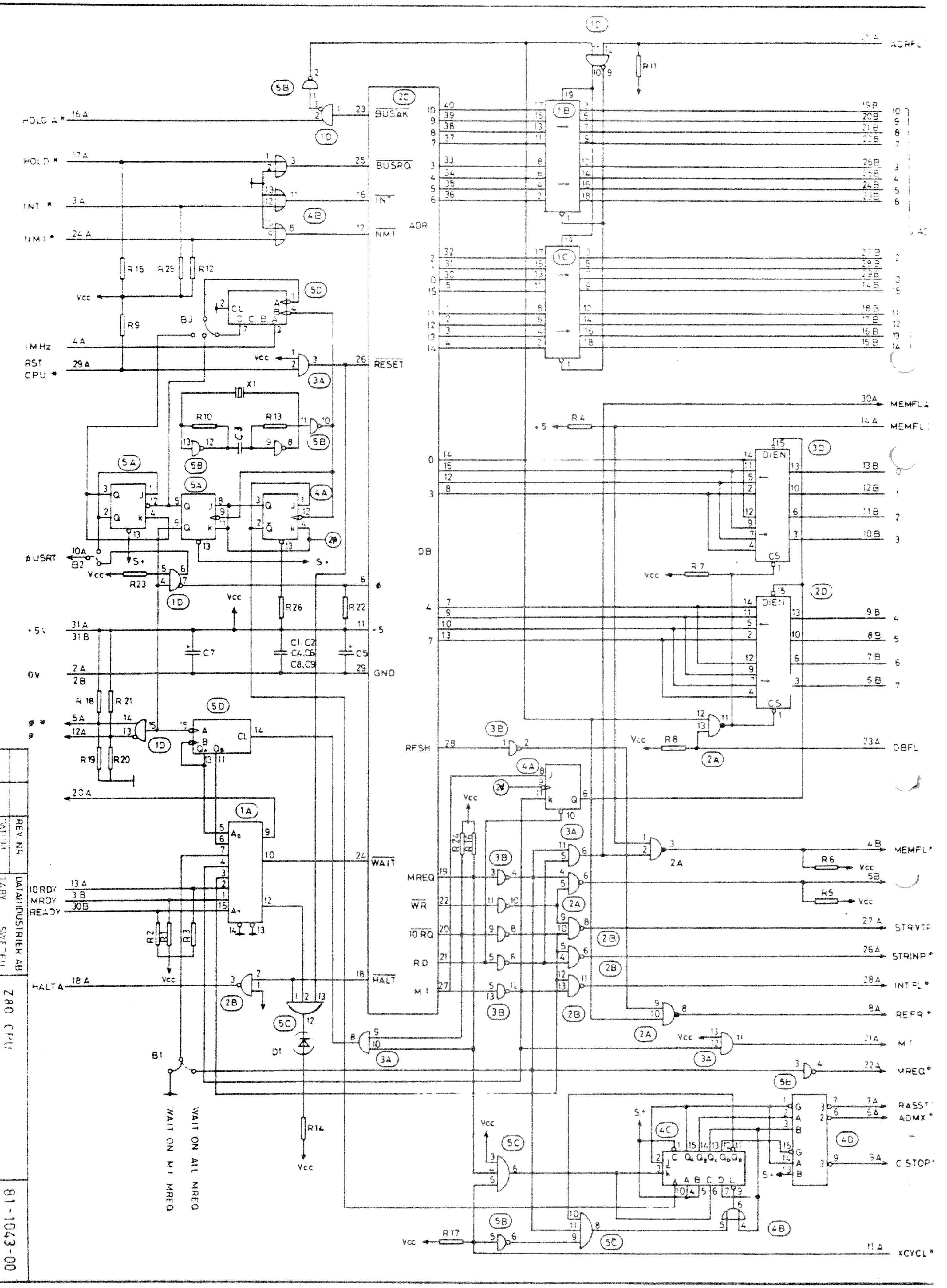
Jumpers for system clock, Ø USRT

X-TAL = 10 MHz and
standard Z 80-CPU

B3/a installed for standard 1043 at shipping.



	A	REV. NR	DATAINDUSTRIER AB	Z80 CPU	82-1043-00
	81.04.09	DATUM	TÄBY SWEDEN		


81-1043-00
Z80 CPU
DATAINDUSTRIER AB
REV NR
HOLD A *
HOLD *
INT *
NMI *
1MHz
RST CPU *
ø USRT
+5V
0V
HALT A
IORDY
MRDY
READY
WAIT ON ALL MREQ
WAIT ON M1 MREQ
BUSAK
BUSRQ
INT
NMI
RESET
WAIT
HALT
GND
ADR
DB
RFSH
MREQ
WR
IORQ
RD
M1
ADRFL
MEMFL
DBFL
STRVTF
STRINP *
INTFL *
REFR *
MREQ *
RASST
ADMX *
C STOP
XCYCL *
DIEN
CS
Vcc
S+