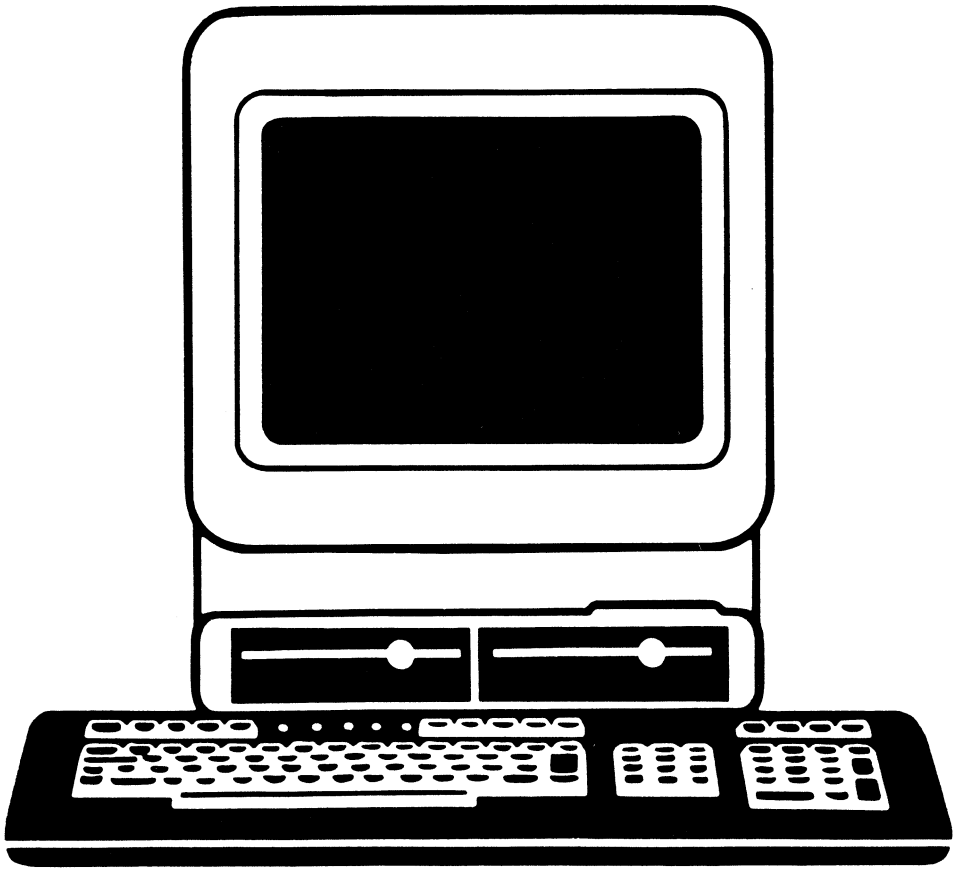
Technical Manual



DTC 2

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1. General

1.0 Introduction

The new Facit DTC 2 series Desk Top Computer is a two part design, consisting of a main unit with electronics, display and disk units, and a separate keyboard.

(Fig. 1.1 View.)

The Desk Top Computer, henceforth referred to as the DTC 2 is primarily a personal computer, derived from the older model DTC 6500 Series. The changes are mostly in design and technology, but there are also some fundamental functional differences.

As you can see from figure 1.1 the DTC 2 is very compact and has a small footprint.

1.1 Configurations

The DTC 2 comprises four basic configurations. These are:

- Twin floppy disk drives with double sided storage (640 Kbytes). 15" monochrome display unit wich presents 24 lines with 80 characters per line or 512 by 240 pixels of high resolution graphics. The monochrome screen uses yellow colour on dark brown background.

- Twin floppy disk drives with double sided storage (640 Kbytes). 14" colour display unit wich presents 24 lines with 80 characters per line or 512 by 240 pixels of high resolution graphics.

- One floppy disk drive with double sided storage (640 Kbytes) plus one Winchester disk drive with 10 Mbytes of storage. 15" monochrome display unit wich presents 24 lines with 80 characters per line or 512 by 240 pixels of high resolution graphics. The monochrome screen uses yellow colour on dark brown background.

- One floppy disk drive with double sided storage (640 Kbytes) plus one Winchester disk drive with 10 Mbytes of storage. 14" colour display unit wich presents 24 lines with 80 characters per line or 512 by 240 pixels of high resolution graphics.

2 Mechanics

2.0 General

As mentioned above the DTC 2 consists of a main unit and a keyboard.

The main unit contains the following main items:

- Chassis
- Power Supply Unit (PSU)
- Monochrome or colour display (CRT)
- CRT circuits
- Floppy and/or winchester disk drives.
- Computer electronics

A brief outline on each of these units is given under respective heading. The keyboard is given a separate heading.

2.1 Chassis

The chassis of the DTC 2 is made of a plastic alloy exept for the backplane, which is made of cast aluminium. The chassis is coated with a conductive layer of paint which screens undesired stray radiation from the computer. The colour of the chassis is an even grey.

The chassis is moulded in one piece except for the back, and the bottom which is bolted to the rest of the main unit. There are openings in the chassis for disk drives and the CRT. The CRT is encased in a housing made of the same plastic as is used for the rest of the computer.

2.2 Power Supply Unit (PSU)

The Power Supply Unit accepts 220 V (ac) and provides the computer with power lines for +12V, +5V, 0V and -12V.

There are two versions of the PSU. One is used in the twin floppy disk drive configuration and the other is used in the winchester disk drive configuration.

2.3 Monochrome or colour display

The monochrome display screen is a 15" CRT with phosphorus yellow signs on a dark brown background. It has an maximum resolution of 512x240 pixels.

The colour display screen is an 14" CRT with RGB picture control. It has a maximum resolution of 512x240 pixels.

2.4 CRT circuitry

The CRT-circuitry provides the CRT with drive voltages and circuits that control the placement of the pixels on the screen according to the information from the computer.

2.5 Floppy and/or winchester disk drives

There are two versions of the DTC 2.

Normally the DTC 2 is equipped with two floppy disk drives with a capacity of 320 or 640 KBytes each.

It is possible to change one of the floppies for an 10 MByte winchester disk drive.

Booth configurations uses so called slimline drives with 5 1/4" format disks. The disk drives are mounted in openings in the front of the main unit.

2.6 Computer electronics

The computer electronics consists of a CPU motherboard (FCPU) with 5 sockets for circuitboard edge connectors. In these the following five boards are connected to the motherboard: Serial In/Out board (FINO), Character Generator board (FCHA), Full Graphics board (FGRA), Mini Floppy Controller board (FMFC) and Winchester Controller board (option).

2.7 Keyboard

The keyboard contains a dedicated microprocessor and the keyswitches enclosed in a low profile moulded plastic box.

The keyboard layout is constructed with four banks of keyswitches containing alphanumeric, numeric, and function keys. There are also six light emitting diodes on the keyboard. Five of these are under program control (BASIC).

There are 12 function keys placed between the alphanumeric and the numeric keybanks. There are six cursor control keys, 4 dedicated funtion keys and 2 programmable function keys among these.

The keys on the keyboard are programmable. The microprocessor in the keyboard sends the codes of the depressed keys to the DTC 2 which decodes them according to the current character set. The keyboard has a keyboard buffer of 64 characters.

2.8 Specifications

- **Processor unit (Motherboard)**

CPU	Z80 A
Word length	8 bit
Clock frequency	3 MHz
Storage, ROM	8 or 16 Kbyte bootstrap loader including test programs.
Storage, RWM	64 Kbytes of dynamic Read and Write memory.
Calendar clock	58167A crystal controlled calendar clock with battery backup.
Sound generator	Piezoelectric speaker driven by hardvare constructed D/A converter.
Operating system	DOS X.XX CP/M 3.0
Connectors	5x64-pole European standard for DTC bus.

- **Serial communications unit (FINO)**

Timer	Z80 CTC
Synchronous comm.	Z80 SIO/2 (V.24 and Network CH.B)
Asynchronous comm.	Z80 DART (Keyboard & printer CH.A)
Connectors	15-pole D-sub for asynchronous transfer of data. 15-pole D-sub for synchronous or asynchronous transfer of data. 2x9-pole D-sub for Connection to local DTC network. 5-pole DIN for conection of keyboard.

- **Character Generator Board (FCHA)**

CRTC	Motorola 6845S CRT controller.
Monochrome screen	15" yellow phosphor pixels on dark brown background.
Colour screen	14" with colours: Red, green, yellow, blue, magenta, cyan, white and black.
Display size	25 lines by 80 characters.
Full graphics	Maximum 512 by 240 (4 colours) pixels. medium resolution 256 by 240 (8 colours) and 240 by 240 (4 colours).
Character size	Character space 10 x 6 pixels Character matrix 9 x 5 pixels
Character range	96+96+64
Refresh rate	60 Hz.

- **Full Graphics Board (FGRA)**

Storage RWM	128 (or 512) Kbytes of dynamic read/write memory. Can be configured as graphics RWM, Disk-RWM or user RWM.
Resolution	240x240 pixels four colours. 256x240 pixels eight colours. 512x240 pixels four colours.

Pictures	One high resolution picture uses 32 Kbytes of RWM. Maximum 4 pictures in 128 KBytes version and 16 in the 512 Kbytes version.

- **Keyboard**

Number of keys	100
Lamps	5
Characters	96+96+64
Keyboard buffer	64 characters
Function keys	26
Processor	Intel 8035
Data transfer	Serial

- **Power Supply**

Supply type	Secondary switched DC/DC converter		
Voltages	Type	1	2
	Input	V	
	Output	5V,	
		+12V,	
		-12V,	
Power		130W	

3. Installation and Operation

See Operating Instructions, chapter on Installation (Chapter 4) and Operation (Chapter 5).

Signals marked with an asterix (*) are active negative.

3.1 Connectors

3.1.1 DTC 2 external connectors

Fig 3.1 Backplane with connectors.

Serial communications connectors CH.A and Ch.B

CH.A (P75)

Pin	Name	Function	Direction
1	+5V		
2	TxD*	Transmit Data	O
3	RxD*	Receive Data	I
4	RTS	Request To Send	O
5	CTS	Clear To Send	I
6,7	Gnd		
8	DCD	Data Carrier Detect	I
9	+12V		
10	-12V		
11	DTR	Data Terminal Ready	O
12	RI	Ring Indicator	I
13			
14			
15			

CH.B (P72)

Pin	Name	Function	Direction
1	+5V		
2	TxD*	Transmit Data	O
3	RxD*	Receive Data	I
4	RTS	Request To Send	O
5	CTS	Clear To Send	I
6,7	Gnd		
8	DCD	Data Carrier Detect	I
9	+12V		
10	-12V		
11	DTR	Data Terminal Ready	O
12	RI	Ring Indicator	I
13	TC	Transmit Clock	O
14	RxC	Receive Clock	I
15	TxC	Transmit Clock(ext.)	I

Network connectors NET.

NET **(P73, P74)**

Pin	Name	Function
3	In	Serial data in
6	Out	Serial data out
7	Gnd	

Mains power connector.

Name	Function
L	Line
N	Neutral
Gnd	

Keyboard connector.

Keyb. (P71)

Pin	Name	Function	Direction
1	TxD	Transmit Data	O
2	RxD	Receive Data	I
3	Gnd		
4	+12V		

DTC 2 Internal connectors

- Pin configuration on DTC 2 internal connectors J20, J30, J40, J50 and J70.

Connector J20.

	Signal	A-pin	B-pin	Signal
	-12V	A1	B1	-12V
TP1	GND	A2	B2	GND
	FGE	A3	B3	IOW*
	IOR*	A4	B4	GL*
	DEN+1	A5	B5	RL*
	D7	A6	B6	RH*
		A7	B7	GH*
		A8	B8	BL*
DATA		A9	B9	SL*
		A10	B10	SH*
		A11	B11	BH*
		A12	B12	SLOW CLOCK
	D0	A13	B13	MAI*
	MA0*	A14	B14	B15
	0V	A15	B15	
	LGL*	A16	B16	
	BRFSH*	A17	B17	
	MRD*	A18	B18	
	DEW*	A19	B19	
	BMRQ*	A20	B20	Buffered address
	VR*	A21	B21	lines
	F3	A22	B22	
	F3*	A23	B23	
	EME	A24	B24	
	RST*	A25	B25	
	GVEN	A26	B26	
	SCG*	A27	B27	
	H6MHZ	A28	B28	
	6MHZ	A29	B29	B0
	H6MHZ*	A30	B30	0V
TP2	VCC	A31	B31	VCC
	+12V	A32	B32	+12V

Connector J30.

	Signal	A-pin	B-pin	Signal
	-12V	A1	B1	-12V
TP1	GND	A2	B2	GND
	KDTR*	A3	B3	HRS*
	FGE	A4	B4	GL*
	DEN+1	A5	B5	RL*
	D7, HBD7	A6	B6	RH*
		A7	B7	GH*
		A8	B8	BL*
DATA		A9	B9	SL*
		A10	B10	SH*
		A11	B11	BH*
		A12	B12	M1*
	D0, HBD0	A13	B13	MAI*
	MA0*	A14	B14	B15
	DIS	A15	B15	
	LXM*	A16	B16	
	BRFSH*	A17	B17	
	MRD*	A18	B18	
	DEW*	A19	B19	
	BMRQ*	A20	B20	Buffered address
	HRC*	A21	B21	lines
	F3	A22	B22	
	F3*	A23	B23	
	EME	A24	B24	
	RST*	A25	B25	
	GVEN	A26	B26	
	FG*	A27	B27	
	H6MHZ	A28	B28	
TP1	GND	A29	B29	B0
	H6MHZ*	A30	B30	ZW*
TP2	VCC	A31	B31	VCC
	+12V	A32	B32	+12V

DTC 2 bus connectors J40, J50.

	Signal	A-pin	B-pin	Signal	
	-12V	A1	B1	-12V	
	GND	A2	B2	GND	
	RES.IN*	A3	B3	XMEMWR*	
	GND	A4	B4	XMEMRD*	
	XINT*	A5	B5	ΦSYST CLOCK	
	D7	A6	B6	GND	
		A7	B7		
		A8	B8		
DATA		A9	B9		
		A10	B10		
		A11	B11		
		A12	B12		
	D0	A13	B13	GND	
	--	A14	B14	A15	
	XRST*	A15	B15		
	INP1*	A16	B16		
	INP0*	A17	B17		
	OUT5*	A18	B18		
	OUT4*	A19	B19		
	OUT3*	A20	B20		ADDR.
	OUT1*	A21	B21		
	OUT0*	A22	B22		
	CS*	A23	B23		
	NMI*	A24	B24		
	INP2*	A25	B25		
	XINPSTB*	A26	B26		
	XOUTPSTB*	A27	B27		
	XM*	A28	B28		
	REFRESH*	A29	B29	A0	
	RDY	A30	B30	MEMRQ*	
	+5V	A31	B31	+5V	
	+12V	A32	B32	+12V	

Connector J70.

	Signal	A-pin	B-pin	Signal
	-12V	A1	B1	-12V
TP1	GND	A2	B2	GND
	KDTR*	A3	B3	RNO
	---	A4	B4	RNC
	---	A5	B5	---
	D7	A6	B6	---
		A7	B7	---
		A8	B8	---
DATA		A9	B9	NRZ*
		A10	B10	ICL*
		A11	B11	---
		A12	B12	---
	D0	A13	B13	---
	---	A14	B14	---
	---	A15	B15	M1*
	INT*	A16	B16	IEO
	---	A17	B17	---
	---	A18	B18	---
	DEW*	A19	B19	D
	IORQ*	A20	B20	S
	Φ	A21	B21	C
	RIN*	A22	B22	RD*
	F3*	A23	B23	Φ/2
	---	A24	B24	---
	RST*	A25	B25	---
	---	A26	B26	---
	---	A27	B27	---
	---	A28	B28	B1
	---	A29	B29	B0
	---	A30	B30	GND
TP2	VCC	A31	B31	VCC
	+12	A32	B32	+12V

4. Block structure

4.0 General

The logical structure of the DTC 2 is best illustrated by a coarse block diagram (figure 2). The diagram shows the main functional blocks and the structure of the DTC 2.

(Fig. 2. Coarse Block diagram.)

Here follows a brief description of the functional blocks in the DTC 2 computer.

4.1 Block description

4.1.1 Central Processing Unit Board (FCPU), (Motherboard)

Central Processing Unit (CPU)

The Central Processing unit in the DTC 2 is the Z80A microprocessor. The CPU is placed on the motherboard of the DTC 2. The data, adress and control signals of the CPU are buffered on the motherboard. This is done to facilitate interfacing between circuit boards that can be plugged into the five edge connectors on the motherboard and the motherboard.

The CPU is clocked by a 3 MHz signal, derived from a 6MHz clock signal that is generated on the FCHA board.

Calendar Clock

The Calendar Clock consists mainly of a programmable clock cicuit (National 58167A). This circuit contains counters, latches and registers which enables the device to save settings and to continue counting in standbye mode. In standbye mode the power drain is extremly low (CMOS) which means that the circuit can be powered from a battery when the DTC 2 is disconnected from the mains power.

The Calendar Clock is clocked by pulses from a crystal oscillator. This oscillator has no connection with the system frequency.

Sound Generator

The Sound Generator consists of a simpel D/A converter. The output from the D/A converter drives a piezoelectric speaker.

Random access memory

The Random Access Memory on the FCPU-board can be divided in two parts. The Read Only Memory part (ROM) which holds a permanent set of programs and the Read/Write Memory part (RWM) wich holds application programs and data.

The ROM contains either 8 Kbytes or 16 Kbytes of memory in a

2764 respectively a 27128 EPROM device. The programs include bootstrap loader and test routines.

The RWM contains 64 Kbytes of memory in 8 64 Kbit dynamic RWM chips (MB8264-15).

4.1.2 In/Out Board (FINO)

Serial Interface circuits

The Serial Interface circuits consists mainly of a Z80 SIO/2 and a Z80 DART.

The SIO/2 is used for synchronous or asynchronous communication with peripheral units. One channel is used for network communication and the other is buffered for V.24 communication with provisions for NRZI treatment of the signals. The V.24 link uses the connector marked CH. B on the DTC 2 backplane.

One port in the DART is used for asynchronous transmission of data primarily to a printer or some such device (CH.A). One port is tied up with communication between the DTC 2 and the keyboard logic. Communication on the Printer interface is tied to the connector marked CH. A on the DTC 2 backplane.

Timer circuit

The Timer circuit consists of a Z80 CTC. This device consists of four programmable counter timers.

The CTC is used to generate clockpulses, derivated from the system clock signal. These are used as transmitter or receiver clock signals for the different communication formats.

One counter in the timer is set up as a bitcounter to be used when the computer is transmitting or receiving data in synchronous mode on CH.A.

Connectors

The connectors for the different communication formats are mounted on the FINO board. They are placed so that they are accessible on the back plane of the main unit when the FINO board is placed in the appropriate connector on the motherboard and this is placed inside the main unit.

The connectors are marked CH. A, CH. B and NET. There are two NET connectors.

The FINO board also contains a Reset switch.

4.1.3 Mini Floppy Control Board (FMFC)

4.1.4 Winchester Disk Drive Control Board

4.1.5 Full Graphics Board (FGRA)

The Full Graphics board consists mainly of one section containing 128 or 512 Kbytes of dynamic RWM and one section containing the logic circuits concerned with generation of the graphic pixel code, which is sent to the video generation circuits on the FCHA board.

Read Write Memory

The RWM-block on the FGRA board consists of 16 64Kbit dynamic RWM devices (MB8264-15) and assorted logic for address decoding and generation. The data lines to and from the RWM are also controlled by signals from the CPU and FCHA boards. The 64Kbit RWM devices are pin compatible with 256Kbit RWM devices. The FGRA board is provided with necessary decoding logic to make it possible to change the 64Kbit RWM devices for 256Kbit devices. If this is done the memory will be expanded to 512 Kbyte on the FGRA board.

Full Graphics Logic

The Full Graphic Logic on the FGRA board reads, translates and sends data stored in RWM to the video logic on the FCHA board as four bit pixel code. The video logic uses this data to generate graphic pictures on the display screen.

4.1.6 Character Generation and Video Logic Board (FCHA)

The Character Generation and Video Logic board consists of five main parts. These are the CRT Controller, the Video RWM, the Attribute RWM, the Character Set RWM and the Video Logic.

CRT Controller

The CRT Controller consists of a Motorola 6845S CRT Controller with assorted buffers and decoding logic.

This device controls the generation of sync pulses, video memory addressing and character line selection.

Video RWM

The Video RWM consists of 2Kbytes of Static RWM (TC5514AP-2) with assorted latches, transcievers and decoding logic.

The Video RWM holds the data that represents one screenfull of information. The data in the video RWM is read to the Character Generator byte by byte. Here it is converted to pixels that are placed on the current character line on the display screen by the Video Logic.

Attribute RWM

The Attribute RWM consists of 2Kbytes of Static RWM (TC5514AP-2) with assorted latches, transcievers and decoding logic.

Each byte in the Attribute memory corresponds to one byte with identical address in the Video memory. The information (display screen codes), stored in the Attribute memory controls the presentation of the data in the video RWM on the display screen. The attribute holds information on colour coding, underline, inverse character, blinking character etc.

Character Set RWM

The Character Set RWM consists of 4Kbytes of static memory in 2 TC5517BP (CMOS) devices. It can be accessed either by the system or by the Video logic.

A character set is placed in the memory when the system is booted. The character set can be defined by the user.

The character set defines the form in which the separate characters are presented on the display screen.

A character selected from the Video memory generates, together with the Attribute code for the same address, an address, which is fed to the Character set RWM. This address generates the pixel code that is to be placed in the currently addressed location on the display screen.

Video Logic

The Video Logic generates RGB signals for the colour display and a video signal with vertical and horisontal synchronisation signals for the monochrome display. It also generates a light level control signal that is fed to the RGB screen. This signal is superimposed on the video signal for the monochrome screen.

The RGB signal that is fed to the video circuits is selected in a Programmable Array Logic (PAL) device. The PAL selects the RGB signals either from the Full Graphics board, or from the Character Generator on the FCHA board.

5. FCPU Board (Motherboard)

5.0 General

The FCPU board is divided in several blocks (see fig 3), with the following functions:

- Z80A microprocessor
- I/O and MEM Select
- RESET, NMI and INT
- Calender Clock
- 8 or 16 Kbyte ROM with control circuits
- 64 Kbytes RWM with control and refresh circuits

5.1 Z80A microprocessor

The Z80A microprocessor controls the transfer of data on the data bus via the address and control buses. It also manipulates the data with logic, aritmetic or bit manipulative operations.

The address bus allows one way transfer. It is buffered and brought to the five edge connectors on the FCPU board. It is also used on the FCPU board both buffered and unbuffered. Buffered address lines address the ROM and RWM and unbuffered lines are used to address the Chip Select Logic and to generate Video RWM select signals.

The data bus is used in an unbuffered version on the FCPU board and it is also available in unbuffered form on connectors J20, J30 and J70. Before it is brought to connectors J40 and J50 it passes an octal bus transciever. Flow direction in the buffer is controlled from I/O and MEM control.

Extended information on the Z80A can be found in Appendix 1 or in the manufacturers data sheets.

5.2 I/O and MEM Select

The I/O and MEM Select consists of four main logic blocks with some additional logic.

The I/O decoding circuitry is enabled when the processor performs an I/O read or write cycle. This is done by decoders which uses the lines A0 through A7 on the address bus in conjunction with the IORQ* and the RD* or WR* signals from the CPU.

The range for the I/O request lies between addresses 0 and 255. Addresses 0 - 31 and 128 - 255 causes external I/O strobes to the motherboard connectors J40 and J50. The

addresses 32 - 127 are reserved for internal I/O units on the motherboard and on devices attached to connectors J20, J30 and J70.

The block named CHIP SEL. LOG. performs the primary decoding of internal and external I/O units. The four most significant bits of the address bus selects, one of the five internal I/O unit chip select signals (V, C, S, D or R), or else it enables the block namned MUX2.

The internal I/O enable signals enable the following units:

- V enables the selector in MUX1.
- C enables the CTC on the FINO board.
- S enables the SIO/2 on the FINO board.
- D enables the DART on the FINO board.
- R enables Calender Clock.

The MUX2 block sets the I/O signals to external units and to a few internal units as well. The signals are selected from the three least significant bits B0 - B2 on the buffered address bus. There are several signals that enable different parts of the MUX2 block. Address line A7 low in conjunction with address lines A4 - A6 high and IORQ* active presets the selectors via the signal IO GATE ENABLE. The exact choice of external chip select is then determined by the RD* and WR* signals from the CPU.

The signals chosen in this way are INP0* -INP2*, XRST* and OUT0* -OUT5*. These are external signals to connectors J40 and J50. Also selected by the same setup are the SOUND, HRS* and HRC*. The XMEMWR* and XOUTPSTB* are selected by WR*, BMRQ and IO GATE ENABLE.

The XINPSTB*, XMEMRD*, DIR and MRD* are selected by RD*, MRQ*, LXM, LXM*, F3* and IO GATE ENABLE.

The MUX2 block also includes the cicuits needed to derivate the system clock F3, F3* and Φ from the 6MHZ signal from the FCHA board.

The MUX 1 block is selected by the IOW* and the V signal from the CHIP SEL. LOG. Block. The outputs are selected by the state of buffered address lines B0-B3. The selector generates four signals. The Light Level (LGL*), Soft Character Generator (SCG*), Latch Enable, or FF Set which sets the sound level in the Sound Generator.

The block marked LATCH, D/A CONVERT. and MEM. SEL. contains a latch, which is enabled by the latch signal from the MUX 1. The latch puts out signals, that controls ROM or RWM selection both on the FCPU and the FGRA boards. The signals ICL and NRZ selects baudrates for the SIO/2 and enables the NRZI mode.

The MEM. SEL. part of the block generates the VR* signal, which is used to generate CAS on the FCPU and FGRA boards.

I/O addresses in the DTC 2.

UNIT	ADDRESS 7 6 5 4 3 2 1 0	FUNCTION	PORT NR. OUT	IN
EXT.BUS CONN.	0 0 0 0 0 0 0 0	INP0*, Input data		0
J40, J50	0 0 0 0 0 0 0 1	INP1*, Input status		1
	0 0 0 0 0 0 1 0	INP2*, Input opt.status		2
	0 0 0 0 0 0 1 1	Optional		3
	0 0 0 0 0 1 0 0	Optional		4
	0 0 0 0 0 1 0 1	SOUND, Sound generator		5
	0 0 0 0 0 1 1 0	Optional		6
	0 0 0 0 0 1 1 1	XRST*, Resets I/O reset		7
	0 0 0 0 0 0 0 0	OUT0*, Output data	0	
	0 0 0 0 0 0 0 1	OUT1*, Outp. Chan. sel.	1	
	0 0 0 0 0 0 1 0	OUT2*, Output command 1	2	
	0 0 0 0 0 0 1 1	OUT3*, Output command 2	3	
	0 0 0 0 0 1 0 0	OUT4*, Output command 3	4	
	0 0 0 0 0 1 0 1	OUT5*, Output command 4	5	
FGRA BOARD	0 0 0 0 0 1 1 0	HRS*, Choose picture	6	
J30	0 0 0 0 0 1 1 1	HRC*, Write colour box	7	
EXT. BUS CONN.		XOUTPSTB*,XINPSTB*	0-31	
DART on FINO	0 0 1 0 X X 0 0	D, PRINT data	32	32
J70	0 0 1 0 X X 0 1	D, PRINT control	33	33
	0 0 1 0 X X 1 0	D, KEYBOARD data	34	34
	0 0 1 0 X X 1 1	D, KEYBOARD control	35	35
NOT USED			36-47	
FCHA, CRTC	0 0 1 1 0 0 0 0	Do not use	48	
J20	0 0 1 1 0 0 0 1	Read addressed register	49	
	0 0 1 1 0 1 0 0	RD/WR mem.map reg.file	52	52
	0 0 1 1 0 1 0 1	RD/WR attribute	53	53
	0 0 1 1 0 1 1 0	RD protect, WR spec. #54	54	54
	0 0 1 1 0 1 1 1	WR syncdelay(soft scroll)	55	
CRTC	0 0 1 1 1 0 0 0	WR reg. address	56	
	0 0 1 1 1 0 0 1	WR addressed reg.	57	
NOT USED			58-59	
	0 0 1 1 1 1 0 0	WR intensity (D0-D4)	60	
	0 0 1 1 1 1 0 1	WR volume (D0-D2)	61	
	0 0 1 1 1 1 1 0	WR character generator	62	
	0 0 1 1 1 1 1 1	WR special #63	63	
SIO/2 ON FINO	0 1 0 0 0 0 0 0	V.24 data	64	64
J70	0 1 0 0 0 0 0 1	V.24 control	65	65
	0 1 0 0 0 0 1 0	NET data	66	66
	0 1 0 0 0 0 1 1	NET control	67	67
NOT USED			68-79	
REAL TIME CLOCK	0 1 0 1 0 0 0 0	RD clock		80
	0 1 0 1 0 0 0 0	WR clock	80	
NOT USED			81-95	
CTC ON FINO	0 1 1 0 X X 0 0	CH 0, V.24 Transmit	96	96
J70	0 1 1 0 X X 0 1	CH 1, V.24 Receive	97	97
	0 1 1 0 X X 1 0	CH 2, PRINTER	98	98
	0 1 1 0 X X 1 1	CH 3, Bit count	99	99
NOT USED			100-127	
EXT. BUS CON.	1 X X X X X X X	XOUTPSTB*,XINPSTB*	128-255	

5.3 RESET, NMI and INT

RESET

RESET of the DTC 2 is generated in three ways:

1. By POWER ON.
2. By letting an external device activate pin 3A on bus connectors J40 and J50.
3. By pressing the button RESET on the backplane of the DTC 2.

A RESET signal generated by one of these methods is sent via the control bus to the CPU, CTC, SIO/2, DART, CRTC and the external bus connectors J40 and J50.

The RESET signal to external units is called XRST*. This signal can also be generated under program control by activating the external device control signal INP7*.

Non Maskable Interrrupt, NMI

The Non Maskable Interrupt request can only reach the CPU from a device attached to the DTC 2 bus connectors J40 or J50.

When the NMI input on the CPU goes low, the CPU will put the address 0066H on the address bus and fetch the next instruction from this location.

Interrupt

The Interrupt function is used in the system by the CTC, SIO/2 and DART devices. There is however an input line provided on the external DTC 2 bus connectors J40 and J50, which is named XINT*. This signal is also connected to the CPU INT input line.

The CTC, SIO/2 and DART are connected in an interrupt priority daisy chain. CTC has the highest and DART the lowest priority. If any of these devices generates an interrupt the CPU asks that the interrupt vector for the interrupting shall be placed on the data bus. The CPU then resumes execution at the address indicated by the interrupt vector given.

5.4 Calendar Clock

The Calendar Clock (CC) consists of a CMOS device from National with device number MM58167A. This unit contains a real time clock driven by a crystal oscillator, with a different frequency from the system clock frequency.

Figure 5.2 Calender Clock Block Diagram.

When the system wants to write to or read from the CC, the CC is enabled by line R from the CHIP SEL. LOG. block.

Data direction is determined by the state of select lines IOR* and IOW*.

The device contains apart from the clock circuits, a number of registers and 56 bits of RWM.

The CC is provided with battery backup, which enables it to continue counting even when the DTC 2 is shut off or disconnected from the power line. The battery carries power for approximately 5 years of use, without external power.

The CC keeps track of Year, Month, Day, Hour, Minute and Second. It has no provision for taking leap years into account.

The 56 bits of CMOS RWM included in the CC is used in the system to store certain preset parameters apart from the clock settings. These parameters include the settings that the user sets in the SETUP-function.

The CC uses the READY signal to inform the CPU when it is ready to read or write data from or to the data bus. RDY places the CPU in an inactive state until it is released, whereupon the CPU can resume processing. For further information see appendix 2 or the manufacturers data sheets.

5.5 ROM and RWM with control logic

ROM

The ROM area contains only ROM chip. This chip can either be an 8 Kbyte 2764 unit or a 16 Kbyte 27128 unit or their equivalent. The address area for the ROM is 0000H to 1FFFH or 3FFFH. This area is addressed by buffered address lines B0 to B13.

Decoding is provided to enable (DIS*, MRD* and BOOT*) the ROM. When the RWM area is addressed the ROM is disabled since they occupy the same address area in parallel. When the ROM is enabled the RWM is disabled by BOOTE.

RWM

The RWM area contains 64 Kbytes of dynamic memory in 8*64 Kbit chips. The DRWM PROT. LOGIC block contains neccesary logic to set RAS* and CAS* signals in time to select row and column addresses from a multiplexer, to the memory latches. Data is read or written depending upon the state of signal W*, which is a derivate of the RD* signal from the CPU. The block also contains logic to refresh the appropriate address when the RFSH* signal from the CPU is active.

The DRWM PROT. LOGIC also makes sure that no accidental read/write is done to the DRWM when any of the following operations are taking place:

- I/O Read/Write to any unit selected by the CHIP SEL. LOGIC. WRPROT signal.
- Video RWM Read/Write. DIS signal from FGRA board.
- External RWM Read/Write. XM* signal from DTC 2 external bus connectors.
- Boot ROM read. BOOTE signal from boot ROM enable logic.

6. FINO Board

6.0 General

The FINO board contains circuits that control communication between the DTC 2 and the external world. All comunication is done over serial links. The FINO board contains logic to support four serial links. The controllers consist of one Serial Input Output device (SIO/2), one Dual Asynchronous Receiver Transmitter device (DART) and one Counter Timer Circuit device (CTC).

Apart from these devices the FINO carries logic to select different clock frequencies for transmitter and receiver clock signals.

There is also one selector that controls whether data transmission and receiving on one channel from the SIO/2 shall follow NRZI protocol or not.

Furthermore there are line drivers/buffers on all Input and Output lines in the communications interfaces.

The CTC, SIO/2 and DART are connected in an interrupt chain as described in section 5.3. Each Interrupt output from the devices are connected to the signal INT*, which is brought to the FCPU board. Also the IEO output on the DART is brought to the FCPU board. The IEI line on the DART is set by the output IEO on the SIO/2. the Input IEI on the SIO/2 is set by the ouput IEO on the CTC and the input IEO on the CTC is permanently set high.

This gives a daisy chained interrupt ladder in which the CTC has the highest priority and the DART has the lowest priority. The daisy chaining is carried through internally in the units. This means that the Timer 0 in the CTC has a higher priority than Timer 1 and so on. This gives a total of 8 units that can generate an interrupt. The CPU responds on an INT* signal by activating first M1* and shortly thereafter IORQ*. The unit with the highest priority will then place the contents of its interrupt vector register on the data bus for the CPU to read. The CPU then resumes execution at the apropriate address.

The FINO also has the RESET Switch mounted on the board. The signal lines from the switch are brought to the edge connector and from there the FCPU board takes control over them. (See section 5.3.

6.1 CTC

The CTC contains four programmable counter timers. They are controlled by the CPU which places necessary data in the registers of each timer when the FINO is initiated.

Channels 0, 1 and 2 has the same input frequency, namely the system frequency divided by two (Φ/2). The input frequency on timer 3 can be selected from the output of Timer 0, or from the Transmitt Clock input on Communications Channel B

(SIO/2 port A).

The output of timer 0 can be selected as Transmit Clock frequency for Communications Channel B (SIO/2 port A).

The output of Timer 1 can be selected as Read Clock frequency for Communications Channel B (SIO/2 port A).

The output from Timer 2 sets the Read Clock (RxC) and the Transmit Clock (TxC) for Communications Channel A (DART port A).

The output from Timer 3 is unused. Timer 3 is used as a counter to keep track of the number of databits received from or transmitted to an external device over Communications Channel B. The timer counts pulses on the Transmit Clock signal line.

6.2 SIO/2

The SIO/2 has two ports which can be set up for synchronous or asynchronous transmission of data. Port A is connected to Communications Channel B on the DTC 2 back plane, and port B is connected to the Connectors marked NET.

6.2.1 Port A

Port A is connected to line drivers and buffers in a conventional V.24 communications setup. The exact pinout of the signals on Communications Channel B can be found in the connector descriptions in Section 3.1.1.

The selector switch between on and off board generated clock signals for Receive Clock (RxC) and transmitt Clock (TxC) is controlled from the FCPU board via the ICL* signal.

The selection of NRZI communications format is done from the FCPU board via the signal NRZ*. This selector shunts the Transmit Data (TxD) and Receive Data (RxD) signals through the NRZI encoder block. For further information on NRZI communications you are referred to Appendix 3.

6.2.2 Port B

Port B is set up to transmit or receive data in serial form over a synchronous communications line (NET) consisting of three wires. These are Out (Transmit Data), In (Receive Data) and Ground. Data is clocked onto the Out line by a clock frequency derivated from the system clock through division by 5. In Port A this frequency is divide by four. This gives us a transmission frequency of 150 KHz.

The same frequency is used to clock data into the port from the In line.

The Pin DCD* on Port B is connected to a signal namned RIN from the FCPU. This line enables the computer to measure how long time the RESET Switch has been depressed.

6.3 DART

The DART contains two ports for asynchronous communication. Port A is connected to Communications Channel A on the DTC 2 back plane. This port is normally used as a printer port.

Port B is connected to the keyboard of the DTC2.

6.3.1 Port A

Port A receives clock pulses for both Transmit Clock (TxC) and Receive Clock (RxC) from the output of Timer 2 in the CTC. The signals to and from the Communications Channel passes line drivers and buffers. These sets the signals to the appropriate level and with appropriate drive capability for V.24 (RS.232) protocol. The exact pinout of the signals on Communications Channel A can be found in the connector descriptions in Section 3.1.1.

6.3.2 Port B

Port B receives its Receive and Transmit Clock signal (RTxC) from a divider setup which takes the 1.5 MHz Φ/2 clock from the FCPU and divides this with 20 to generate a 75 KHz signal.

The Receive Data (RxD) and Transmit Data (TxD) signals are brought to the keyboard connector through a line driver and a buffer. The Ring Indicator input (RI*) line is activated by the signal DEW*, which is generated on the FCHA board. This signal is a derivate of the Vertical Sync. signal (VS).

The Data Transmission output (DTR*) sets the line KDTR*, to the PAL circuit on the FGRA board.

7. FGRA Board

7.0 General

The FGRA board stores high resolution pictures in 128 Kbytes of RWM. It also controls the transmission of the data in the picture memory to the Video Generation Logic on the FCHA board. The data in the memory can also be read back by the CPU, which makes it possible to use the High Resolution picture memory as user memory or as a RWM-Floppy.

The FGRA board consists of four main blocks. These are:

- INPUT/OUTPUT TIMING and CONTROL.
- PAL decoder.
- Full Graphics DRWM with address selectors and data transfer control cicuits.
- COLOUR BOX with RWM for colour decoding and RWM for ful graphics DRWM addressing.

Fig. 7.1. FGRA, Full Graphics Board.

7.1 INPUT/OUTPUT TIMING and CONTROL

The INPUT/OUTPUT TIMING and CONTROL block can be subdivided in four parts.

The INPUT TIMING and CONTROL block buffers the 6 MHz clock signal from the FCHA board. It also generates a signal (HI3*), which clocks the Refresh signal (BRFSH*) and the Memory Read (MRD*) signal from the FCPU. The clocked MRD* signal selects between the upper and lower 64 Kbytes of the RWM when the CPU reads or writes data.

The Shift Register generates the two most significant address bits to the controlling PROM device. It also generates the Select signal (FGE) to the PAL device on the FCHA board.

The OUTPUT TIMING and CONTROL block in conjunction with the controlling 32 byte PROM circuit generates signals that control RWM address selection with signals MUX A and MUX B. It also generates RAS* and CAS* signals and it blocks the CAS* when the CPU initiates a memory Refresh by activating the RFSH* signal.

This block also generates a signal (COUNT DOWN) which generates one of the four possible addresses that can be selected to the FGRA memory. The signal clocks a 15 bit shift register to shape the address.

Further signals generated by this block selects and directs data into the RWM during Write cycles and to the CPU databus or the Picture Pixel encoder during Read cycles.

7.2 PAL decoder

The PAL decoder (Programmable Array Logic) generates three signals, DIS, MUX and HRE. The input signals to the PAL include buffered address bits B11 to B15, M1* from the CPU, LXM*, KDTR* from port B of the DART (keyboard), EME from the FCHA board and a clock signal.

The FG signal from the FCPU enables the PAL.

The DIS signal disables the memory on the FCPU board when active.

The MUX signal selects addressbits M12 to M18. These consists either of address bits B12 to B15 and bits F15 to F18 (these last 4 bits are latched in from the buffered databus bits HBD7 to HBD4), else the address bits M12-M18 are selected from 2 64 bit RWM devices. The output from these is selected by the same signals as above but the Read signal (MAO*) is generated by the FCHA board wheras the latching signal (HRS*) in the first case is generated by the FCPU board.

7.3 Full Graphics DRWM (128 Kbytes) with address control and pixel selection

The DRWM block contains 16x64 Kbit DRWM devices. These can be exchanged for 16x256 Kbit DRWM devices since they are pin compatible with the 64 kbit devices. Pin 1 on the 64 Kbit devices is unused but on the 256 Kbit devices, pin 1 is address line 8 (A8).

The Full Graphics DRWM accepts data from the buffered data bus and relinquishes the data either to the CPU data bus or to the pixel encoding logic. This logic sends pixel code to the Colour Box on lines PX0 to PX3.

7.3.1 DRWM block

The DRWM is divided in two blocks of 64 Kbytes. A Read or Write instruction addresses both the high and the low memory block at the same time.

The Data Read Select circuits makes sure that only the desired data is either placed on the data bus to the FCPU or sent to the pixel encoder.

The Data Write Select circuits places the data in the proper memory block during a memory write instruction cycle.

The DRWM CAS* and RAS* addresses are selected from four different sources by a set of 4 to 1 multiplexers. The multiplexer therefor can select address 0,1 2 or 3.

The multiplexer control signals MUXA and MUXB are generated by the INPUT/OUTPUT logic on the FGRA board. Alternate Address 0 and 2 are partially generated by the signal COUNT ↓. Partially they are selected from the buffered data

bus signals HBD0 to HBD3 via a latch controlled by the HRS* signal from the FCPU board.

Alternate Addresses 1 and 3 are selected from the buffered address bus signals B1 to B11 and the signals M12 to M18.

The address signals with the highest priority M17 and M18 are used to select address line A8 into the DRWM block. This line has a function only if the 256 Kbits DRWM devices are installed.

7.3.2 Pixel encoder logic

The pixel encoder logic consists of two 8 bit latches and four 8 bit Parallel in/Serial out shift registers.

When data is read from the DRWM, it is read into the shift registers. Two read cycles are needed to fill the registers.

The data in the registers is then clocked out on the pixel data lines PX0 to PX3. These lines are channeled to a multiplexer in the Colour Box block.

7.4 COLOUR BOX and RWM blocks

The Colour Box decodes the pixel data into RGB code acceptable by the video control logic. The decoding of the pixel data is done in two 64 bit RWM devices.

7.4.1 Multiplexer

The multiplexer either selects the pixel code or addresses from the buffered address bus, lines B8 to B11.

The address lines are selected during a Memory Write cycle. During this data is written into the RWM units. The data is later used to generate the RGB-code.

The direction of transfer in the RWM is selected by the HRC* signal from the FCPU board.

The Pixel data lines are selected during a Memory Read cycle. They serve as address lines to place appropriate data on the RGB-lines.

7.4.2 RWM units

There are two 64 bit RWM units. Each of them can therefore hold 16x4 bit nybbles where each nybble is a RGB-code. This means that 16 colours at most can be generated without rewriting the information stored in these RWM units. The data stored in the RWM can be different in the two blocks since they have separate Data In lines. The Data Out lines are referred to as RGBSL(ow) and RGBSH(igh). There are four lines out from each memory unit. The lines are active low.

8. FCHA Board

8.0 General

The FCHA board contains circuits that control the generation of characters and pictures on the display screen (CRT). The board consists of the following main blocks:

- CRT Controller with decoding circuitry.
- Data Bus Isolator and Multiplexer Block.
- I/O Strobe Block.
- Video and Attribute RWM with address selector and data direction control circuits.
- Character Generation Logic.
- Soft Character RWM.
- Pixel code selector and PAL decoder.
- Video Control circuits.

Fig 8.1. FCHA, Character Generator and Video Controller.

8.1 CRT Controller

The CRT Controller consists of a Motorola 6845S CRTC device. Chip Select, Read/Write and Enable signals are generated directly on the FCHA board. Buffered address lines B0 to B7 in conjunction with IOR* and IOW* are used for this purpose.

The CRTC is initiated when the DTC 2 is booted. This means that appropriate data is written into the registers in the CRTC. This data controls the generation of addresses, and sync signals.

The CRT Controller generates Video and Attribute memory address signals for the Video display refresh generation. It also selects the current character matrix row to be displayed on the current character line. This is done by the signals RA0 to RA3. The currently displayed video line is selected by the signals LA0 to LA10.

Further information on the 6845 device can be found in the manufacturers data sheets.

The Horisontal Sync signal (HS), from the CRTC clocks a programmable 8 bit register with the Vertical Sync signal (VS) as data input. The register is set up with data from the CBD0-7 data bus. The Output delivers the Vertical Sync (VS) pulses used in the Video Controller block.

The VS signal also generates the FLSHCLK, SYNC* and DEW* signals. The DEW* signal synchronizies the Picture frame start on the FCHA and the FGRA boards. SYNC* is used by the

Video Controller logic to clock the RGB signals to the Display circuits.

8.2 Attribute Data Bus Isolator and Multiplexer Block

The Data Bus Isolator block controls the data flow between the FCPU data bus and the Attibute memory during FCPU Read or Write cycles. Data is written into the Attribute memory from the buffered (CBD0-7) data bus via the Attribute Bata bus (ATD0-7). Data is read from the memory to the FCPU data bus (D0-7) via ATD0-7. Data direction and control during FCPU read and write cycles are generated by signals MRD*, BMRQ, AMI* and AMO*.

A section of this block is dedicated to generation of early write signals to the Write pins on the Video and Attribute memory devices.

8.3 I/O Strobe Block

The I/O Strobe block generates a number of I/O control signals. It also contains a data bus buffer with data bus signals CBD0 to CBD7 as output signals.

The Strobe section generates Attribute Read and Write strobes (AMI*, AMO*) as well as a number of other signals, among which are the Read and Write Memory Map signals (MAI*, MAO*). The strobes are generated in a dual 1-4 selector, which is enabled by address lines B2 to B7 and IOW* and IOR*. Bits B0 and B1 are used as data input to the selector.

This set up generates I/O address 52H to 55H in Read and Write configuration.

I/O address signals STI* and STO* enables an address latch, which generates strobe signals TXOFF, 40 and EME. The Input to the latch is taken from data lines D0-D2 and D7 on the buffered data bus.

8.4 Video and Attribute RWM block

The Video and Attributes RWM block stores the data that is currently displayed on the screen. The data is read into the block from the FCPU. The CRTC controls the output of data to the Character Generation Logic.

8.4.1 Video and Attribute RWM

The Video and Attributes RWM consists of two identical blocks of 2x2x4x1 Kbytes of static RWM devices (TC15514AP-2). The memory is addressed from the FCPU during data Read or Write cycles by the signals BMRQ, BRFSH* and VR* plus clock CI3. These signals generate the select signals BMRQ*, SEL and CPU*. The address is sent to a multiplexer, which selects buffered address lines B1 to B10 with the signal SEL. Data to either of the Video RWM blocks is fetched directly from the data bus, while data to the Attribute RWM first is passed

through a buffer and a multiplexer before it reaches the Attribute RWM via signal lines ATD0 to ATD7.

The data busses are bidirectional so that the CPU can both Read data from and Write data to the Video and Attribute memories.

During Video refresh cycles the address to the Video and Attribute memory is selected from address lines LA1 to LA10. These are generated by the CRTC device. The address lines address locations in all four blocks of the video and Attribute RWM at the same time. A selection of which RWM block that shall deliver data to the Tx DATA and Tx ATT data lines is done in a set of four latches and Flip Flops. The selection is primarily determined by the state of signals LA0 and LA0* from the CRTC. The latches are controlled by the signal CPU*.

8.4.2 Attribute Handler

There are two versions of the Attribute handler, which generates the Attribute code signals FLP, ULP, F2P-F4P, B5P-B7P and control signals E5P, E6P, and THP.

In version one the signals are generated by a set of dipswitches and a binary counter. In this case the Background colour signals are all low which generates a black back ground on the screen. Signals THP, FLP and ULP are also permanently disabled. The Foreground colour signals can however generate a limited number of colours depending on clock signal DEN+3 and data signal 40 from an address latch in the I/O strobe block.

In version two the dipswitches etc. from version one are replaced by the customs designed device ZY40033, in which case this unit controls the generation of the Attribute signals including the control signals E5P, E6P and THP. Input data to the customer chip consists of the Tx ATT data lines from the Attribute RWM and control signals CLKP, 40 and DEN+3.

8.5 Character Generation Logic (CGL)

The CGL block generates the addresses for the Soft Character Generator memory and it also accepts the Character matrix data and transforms it to serial dot data. This data is transmitted to the Video Logic together with the RGB Backround and Foreground data from the Attribute Handler.

The CGL also includes a crystal oscillator wich generates video and system clock signals.

8.5.1 SCG address generator

The SCG address Generator accepts data from the Video RWM and latches this on to the CGA4 to CGA11 bits of the SCG adress bus. The Remaining address lines CGA0 to CGA3 are generated in a PROM device which is addressed by the RA0 to RA3 and FLSHCLK from the CRTC. These lines address the PROM address

lines A0 to A3 and A6. The remaining address lines A4, A5, A7 and A8 are generated by the Attribute handler. they represents signals ULP, FLP, E5P and E6P. The PROM is enabled by signal THP from the Attribute Handler.

8.5.2 Dot and RGB data generation

The five data bits from the Soft Character RWM, which represents the five bits in one row of the character matrix for one character, are placed in a parallel in/serial out shift register. The DOT signal forms, together with the decoded Attribute data the RGB-code for both background and foreground colour generation. This data is clocked out to form the complete DOT generation signal to the PAL decoder.

8.5.3 Crystal Clock

The Crystal Clock generates a 12 MHz signal. This signal is used to clock the Video circuits together with a second 6 MHz signal. This is derived from the 12 MHz signal in a binary counter. The 6 MHz Clock signal is fed to the FCPU where it is used to generate the System Clock signal (Φ) of 3 MHz.

8.6 Soft Character RWM

The Soft Character Generator contains data, which when properly addressed will yield the dot matrix of each character availible in the DTC 2 character set.

The Soft Character Generator consists of 2x2 Kbytes of static RWM, a 12 bit output multiplexer and a buffer. The RWM (TC5517BP or similar) has the same pin configuration as a EPROM 2716 device.

8.6.1 Write Soft Character Generator (SCG)

Data is written into the SCG from the buffered data bus lines CBD0 to CBD7. The address is built up from address bus lines B8 to B15 and the lower 4 bits are generated by a binary counter.

The multiplexer is set to select the Write address when the signal TXOFF* is active. When signal SCG* from the FCPU is active data is written into the memory.

CLKP* and TXOFF* enables the Soft Character memory.

8.6.2 Read Soft Character Generator (SCG)

Data is read from the SCG when SCG* and TXOFF* are inactive. The address is then constructed from the data read from the currently addressed location in the Video RWM and the Attribute RWM. This information builds up address lines CGA0 to CGA11. The data out from the SCG uses the five Least Significant Bits of the data bus, which are strobed into a shift register in the Character Generation Logic block. The five (5) data bits represent one row in the character matrix for one character.

8.7 RGB-code selector and PAL decoder

The RGB-code selector and PAL decoder consists of a latch, a multiplexer and a PAL device. Together they generate the R*, G*, B* and S* signals that make up the code to the Video Logic.

8.7.1 RGB code selector

The RGB-code selector consists of the abovementioned latch and the multiplexer. The input to the latch consists of the two sets of RGB-code generated on the FGRA board. These are set in the latch and placed on the inputs of the multiplexer. The multiplexer simply switches between these two code sets with a frequency of 6 MHZ.

The code thus selected is placed on four of the inputs to the PAL device.

8.7.2 PAL decoder

The PAL device generates the appropriate RGB code depending on whether it is set to accept code from the FGRA board or from the Character Generation Logic on the FCHA board.

The selection is carried out by the FGE signal and the 12 MHz clock signal.

The input signals from the FCHA board are DOT, RGB Background (3) and RGB Foreground (3).

The output signals are R*, G*, B* and Y*.

8.8 Video Control circuits

The Video Control Block controls the final shaping of video and RGB signals to monochrome or colour display circuits.

The block consists of one octal bus driver and three simple digital to analog conversion units.

8.8.1 RGB signal

The octal bus driver boosts the horisontal and vertical sync signals (HS and VS) as well as the SYNC* signal. The SYNC* signal is delayed in the driver by letting it pass through the driver twice. Also the three RGB signals from the PAL device is passed through the driver.

The R, G, B and CSYNC* signals are availible at the RGB connector P23. A fifth signal called LGT is also availible here. This signal is generated in a D/A converter from the five least significant bits of the buffered data bus.

The signals are latched by the LGL* (Light Level) from the FCPU board. After the latch the signals are buffered and drives a transistor arrangement, which generates the LGT signal at P23.

8.8.2 Video signal

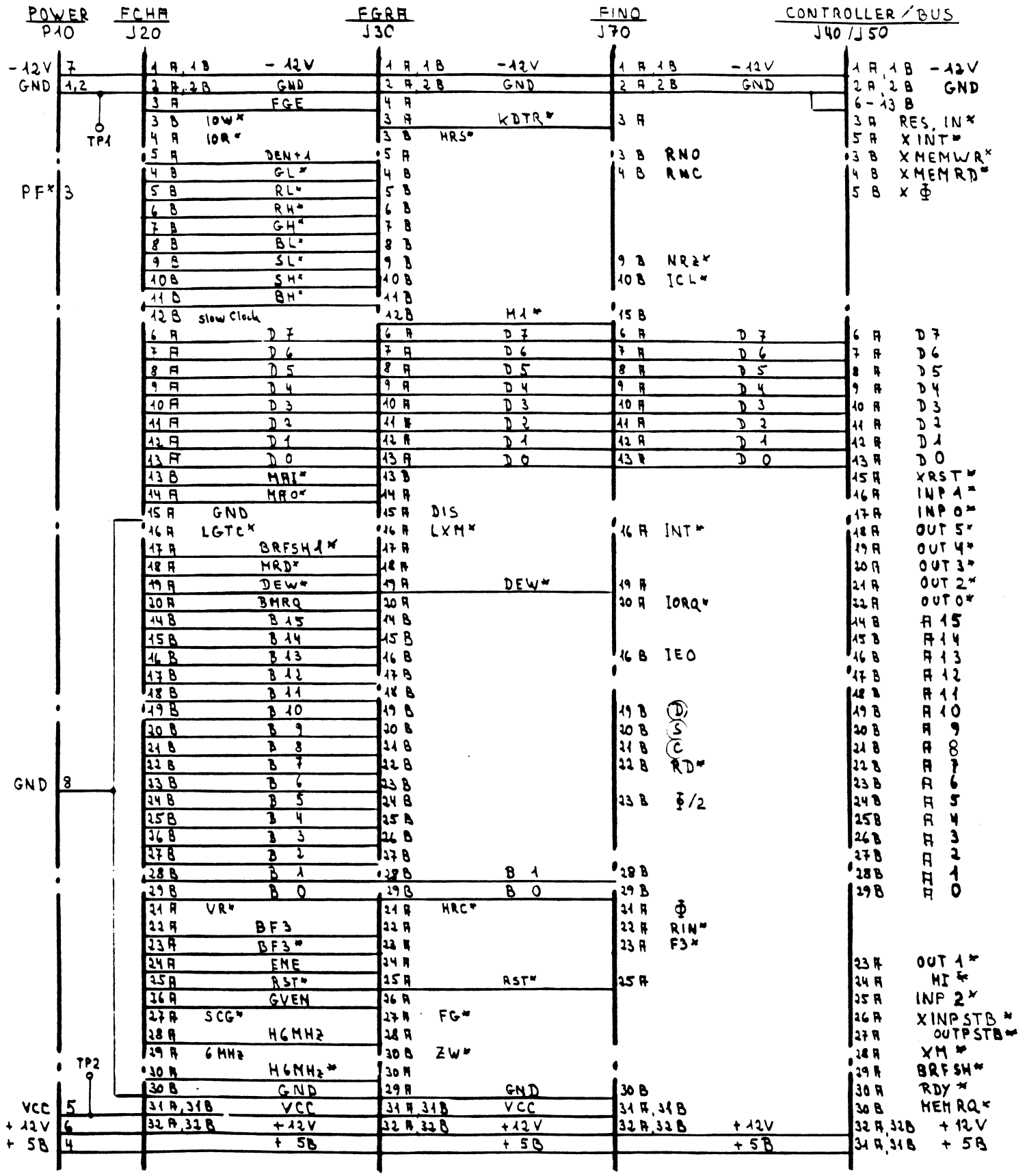
The R*, G* and B* signals and the Y* signal also pass through another driver to a simple D/A converter, which mixes the signals into one. This signal drives a transistor amplifier. The signal VIDEO from this amplifier is delivered at the Monochrome Video Connector P22.

The Video Connector also carries the signals VS* and HS*.

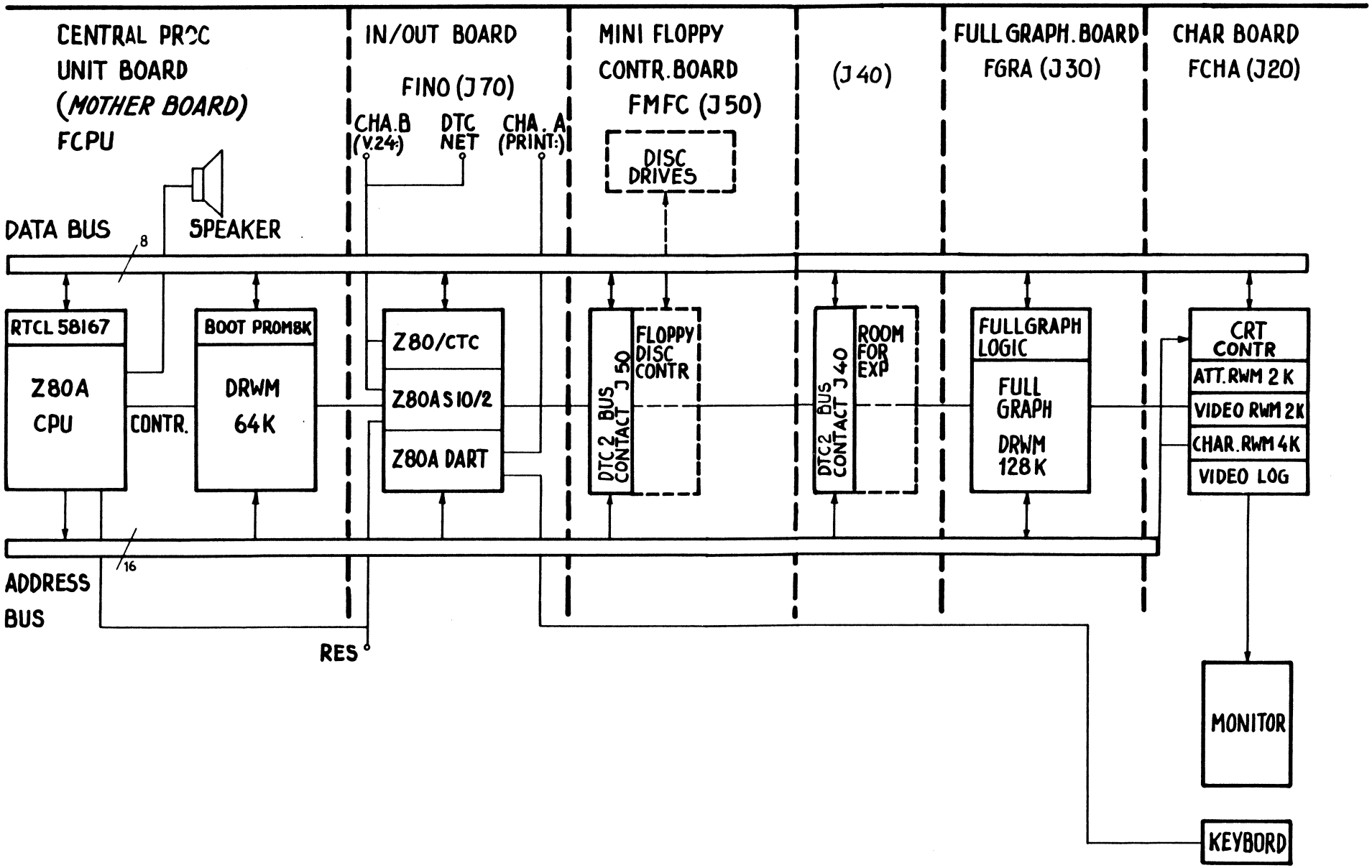
The strength of the VIDEO signal can be decreased by a signal from a D/A converter.

This D/A converter consists of a resistor net on the base of the transistor. By selecting various configurations in the resistor net the VIDEO signal will be forced to different signal strength levels.

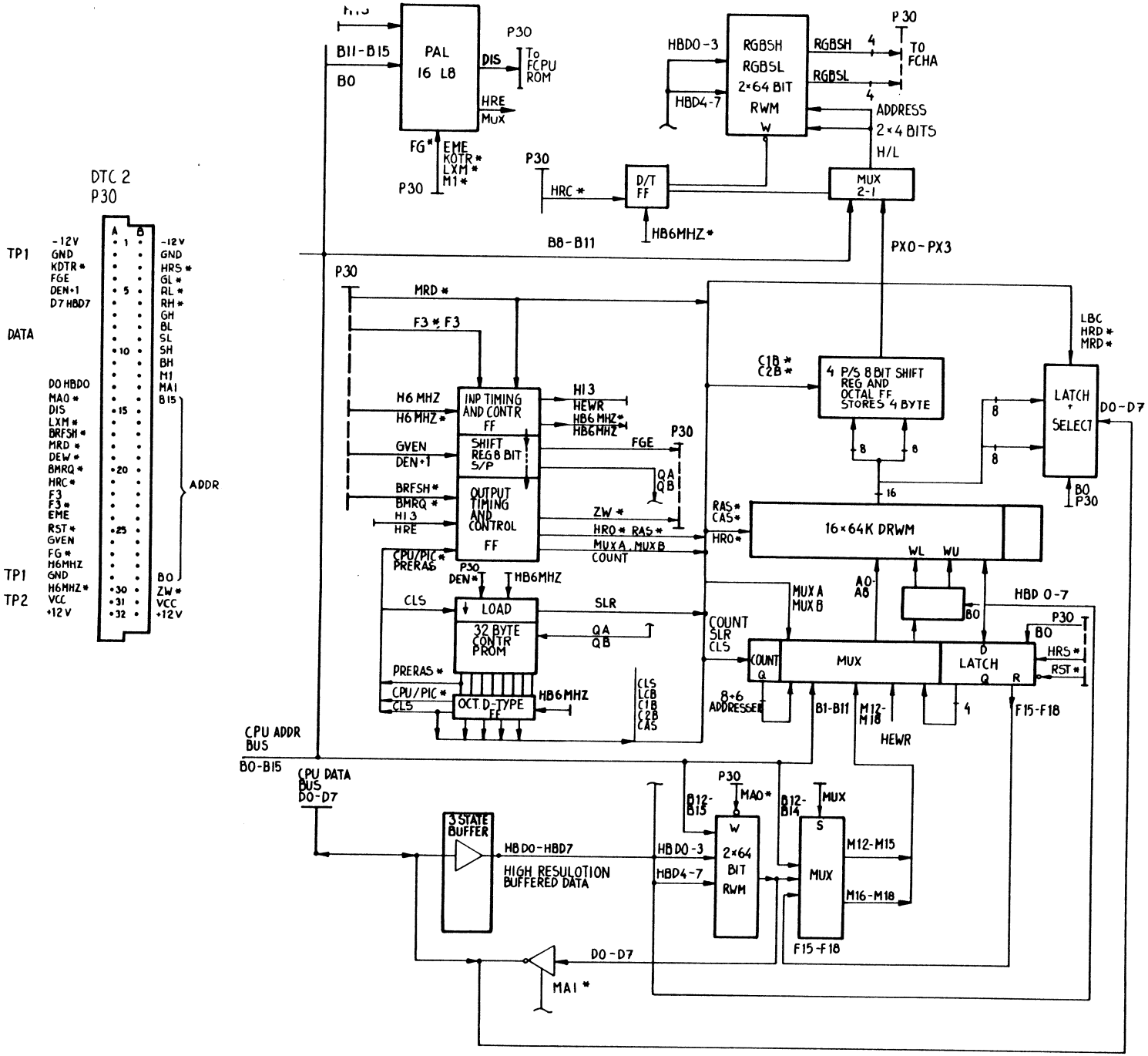
The setting is determined in the same way as in the D/A converter for the RGB signal. That is the five least significant bits of the buffered data bus are latched by the LGL* signal from the FCPU. After the latch the signal are put through a buffer into the resistor net.



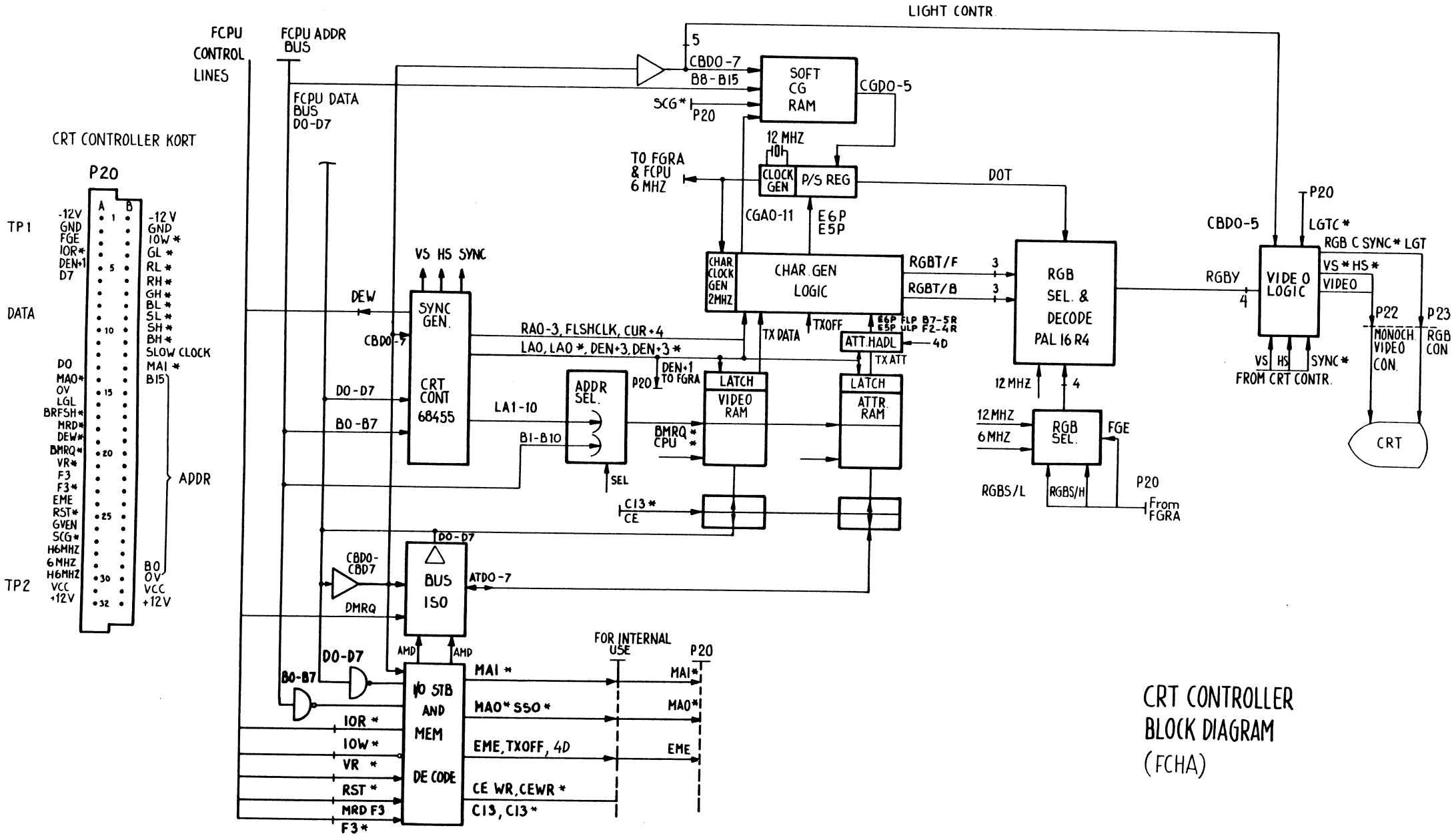
FCPU - internal connections



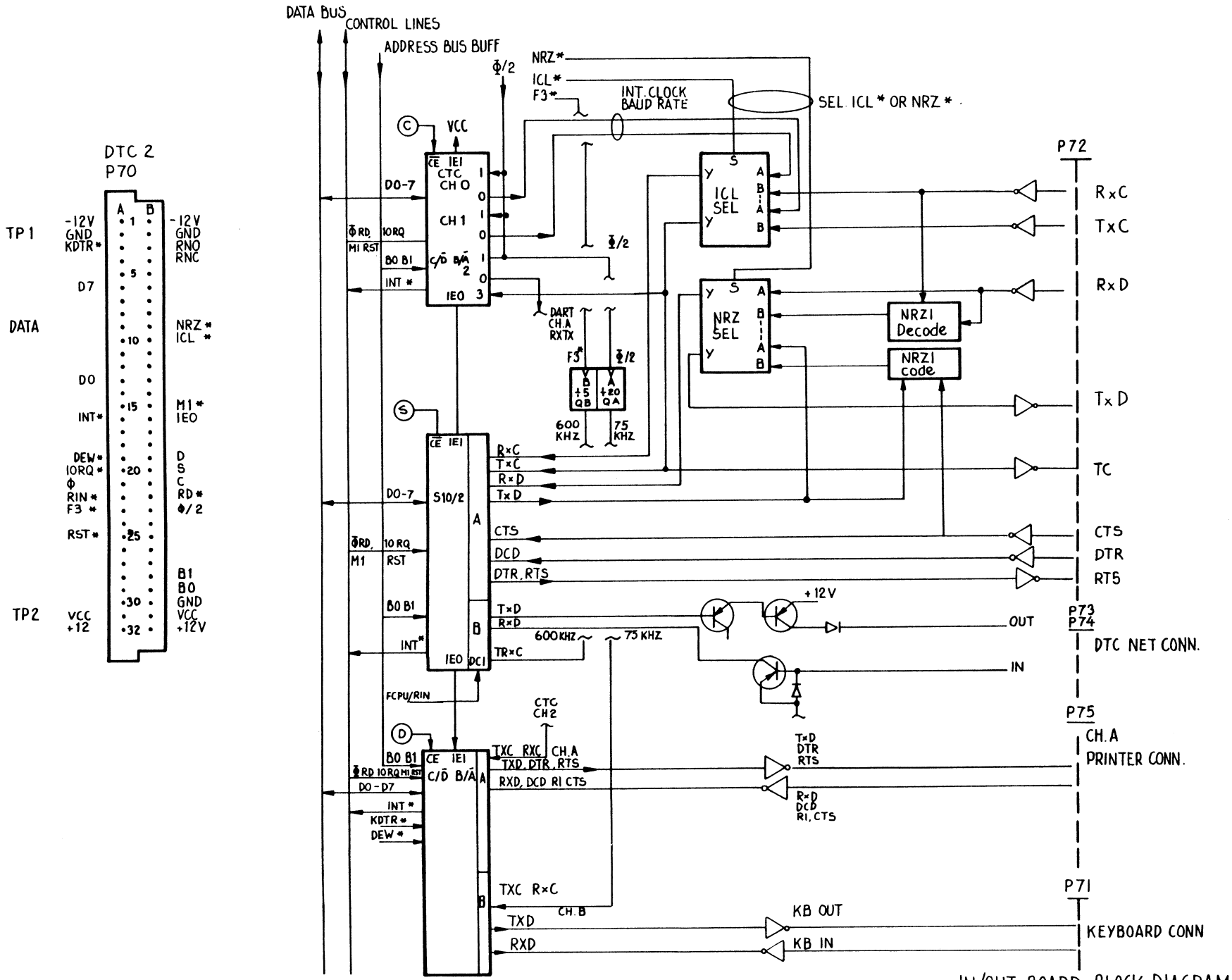
DTC 2 BLOCK DIAGRAM



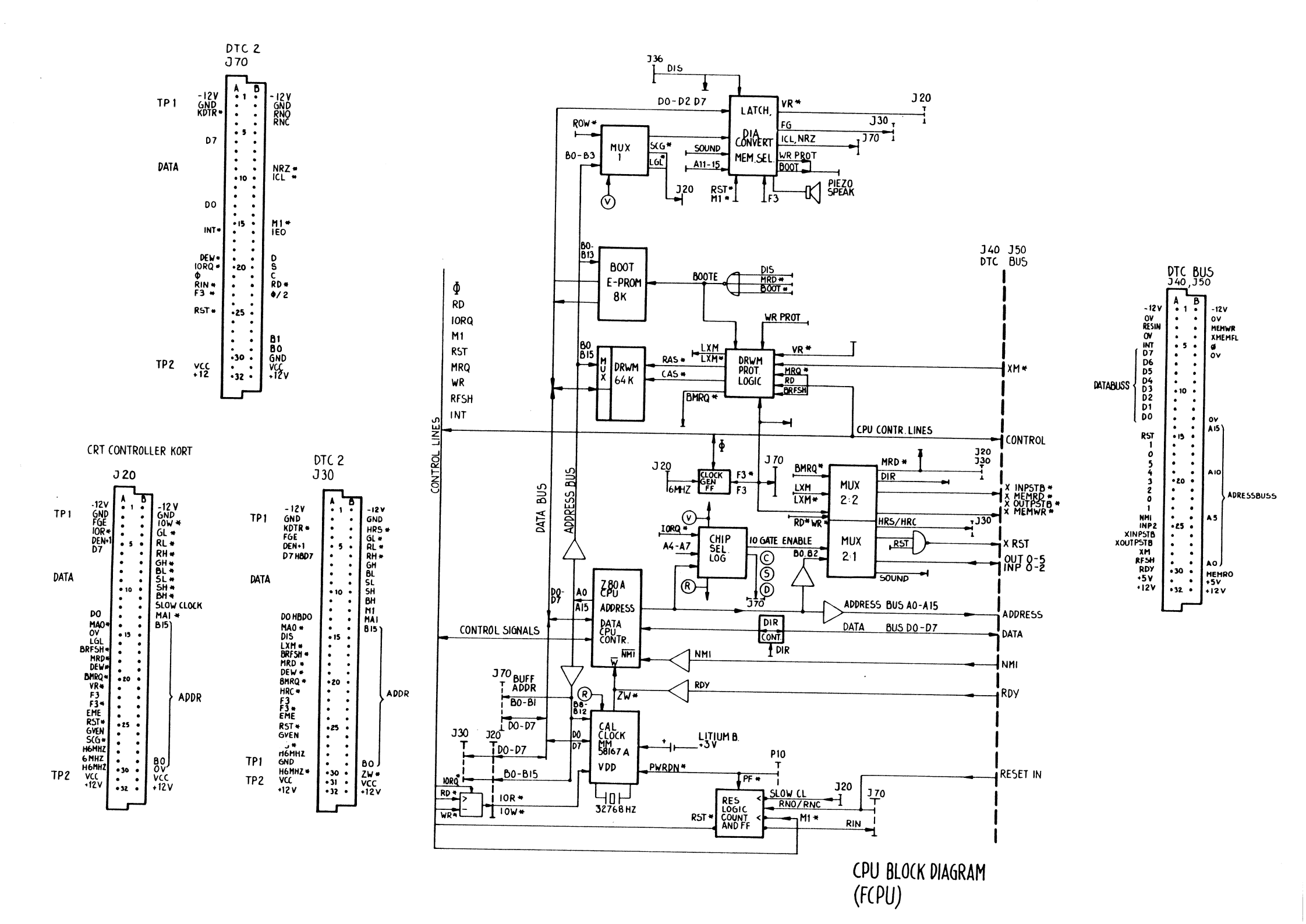
FULL GRAPHICS BOARD BLOCK DIAGRAM (FGRA)



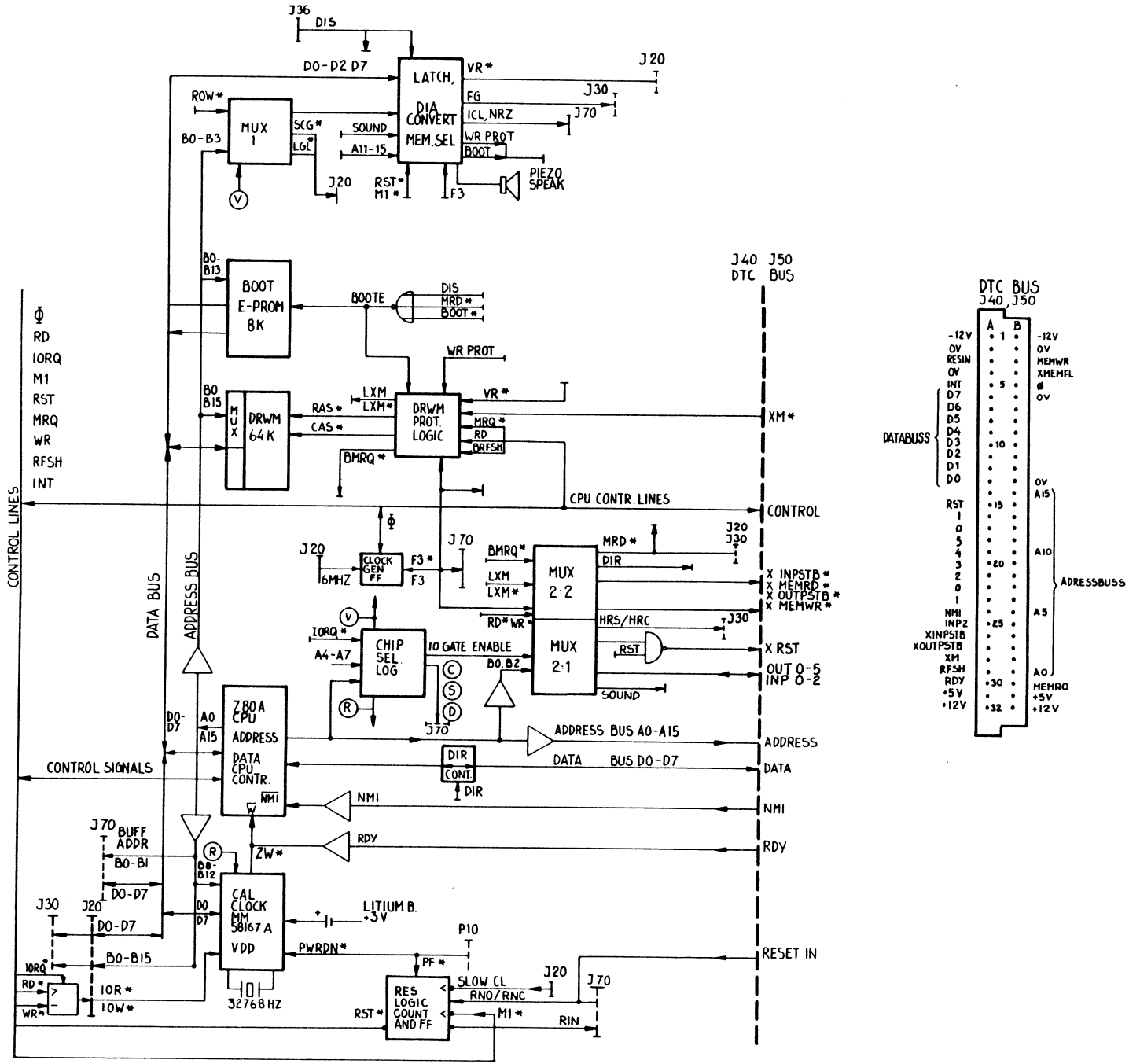
CRT CONTROLLER BLOCK DIAGRAM (FCHA)



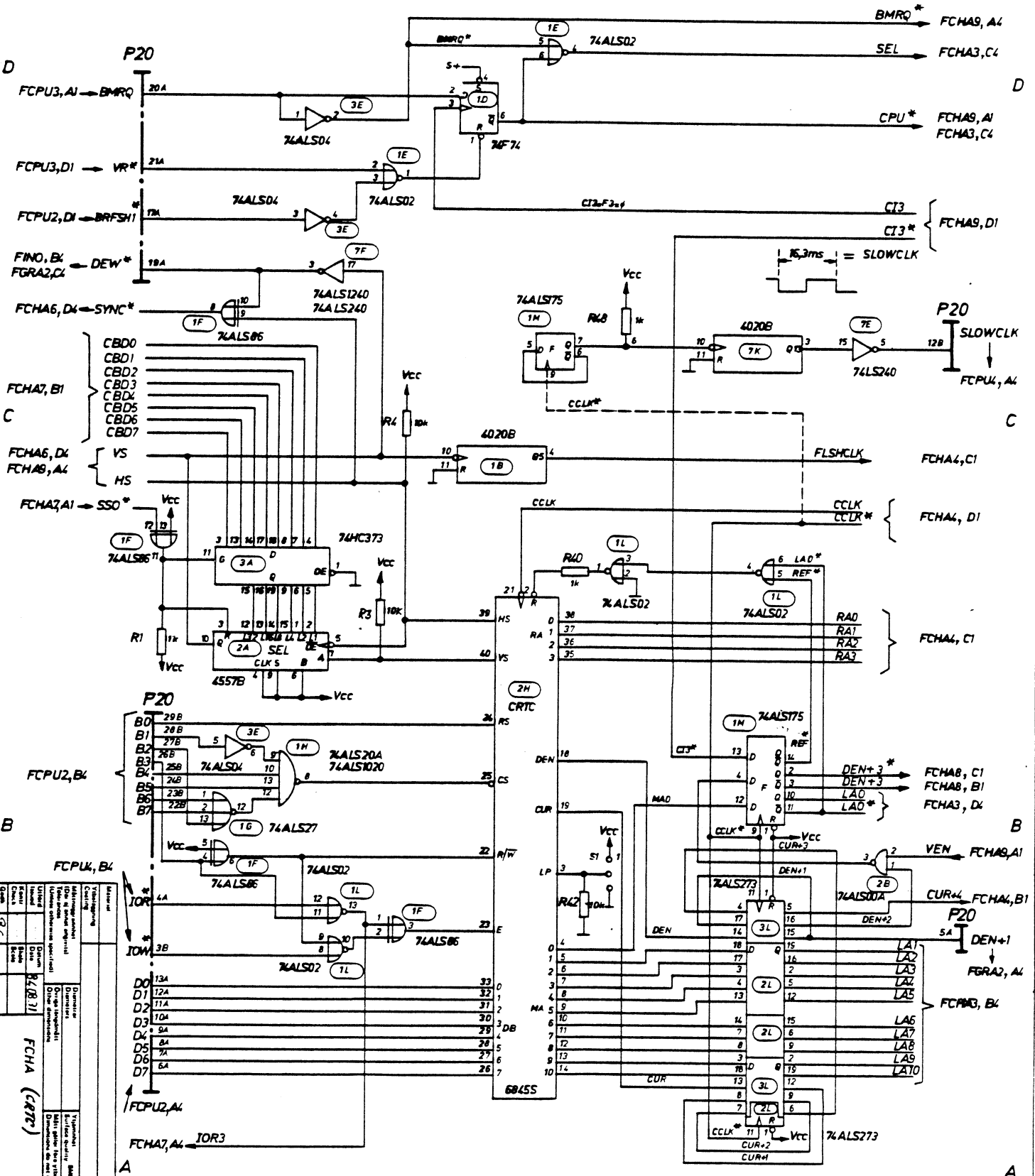
IN/OUT BOARD BLOCK DIAGRAM
(FINO)

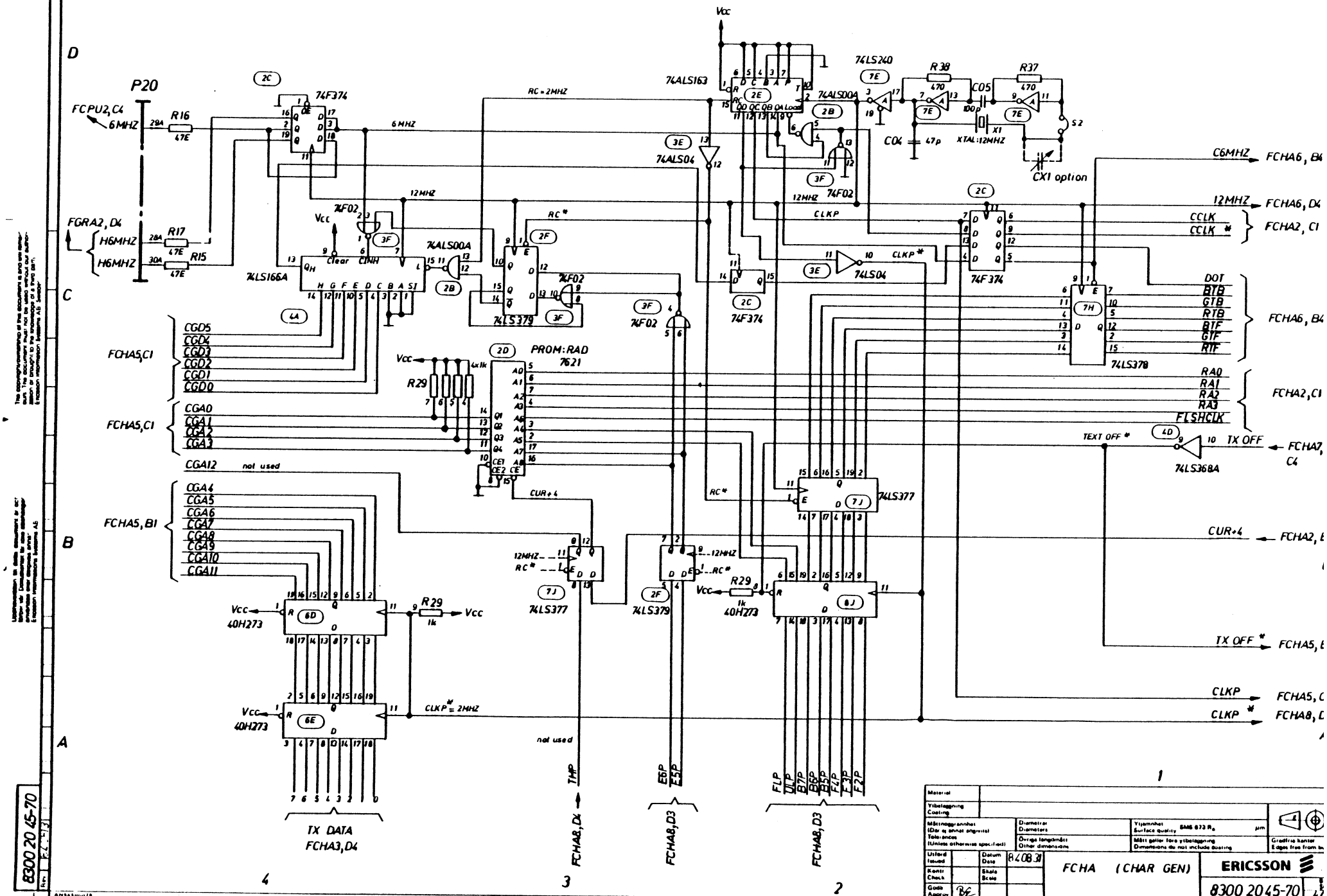


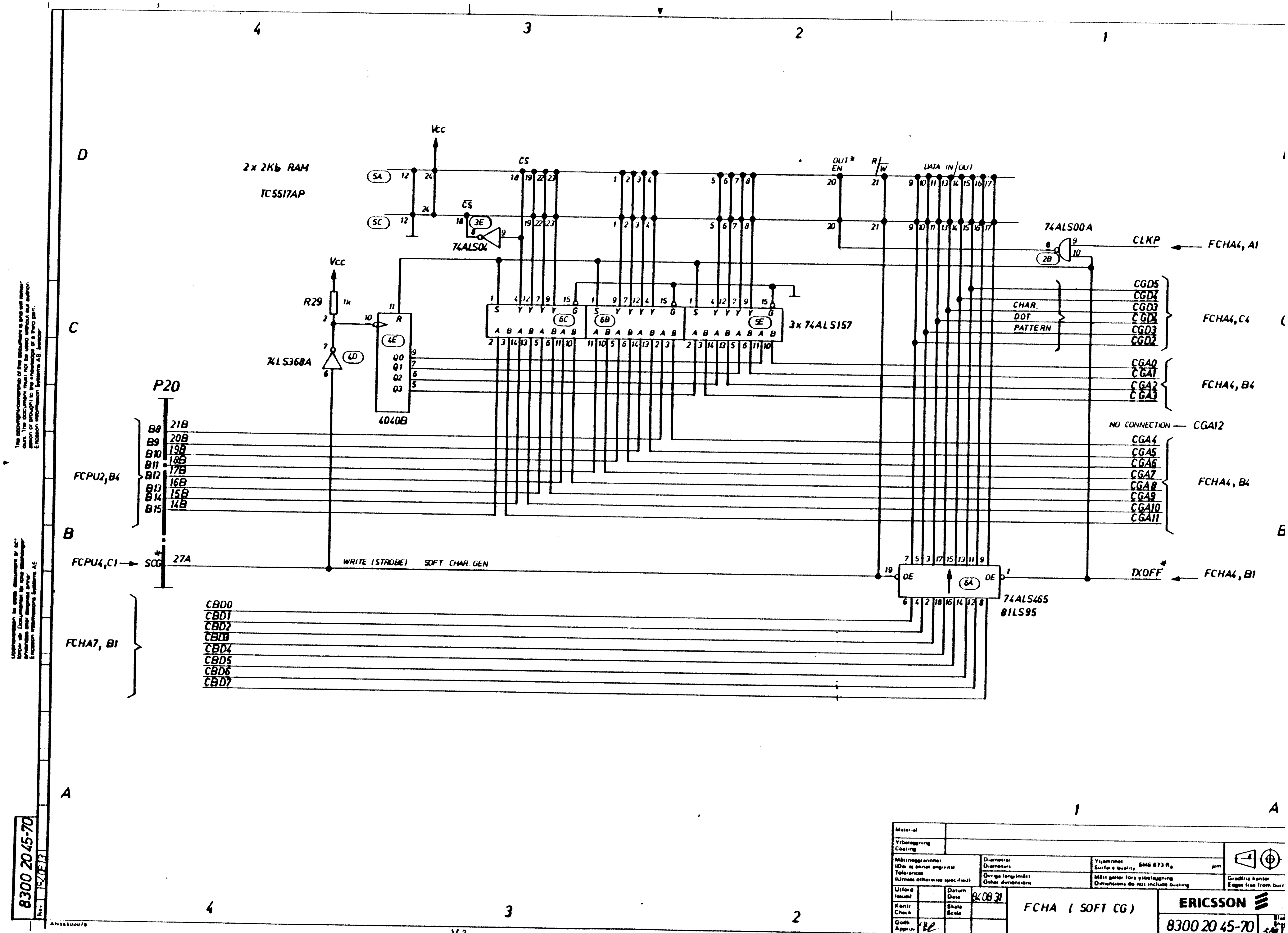
CPU BLOCK DIAGRAM
(FCPU)

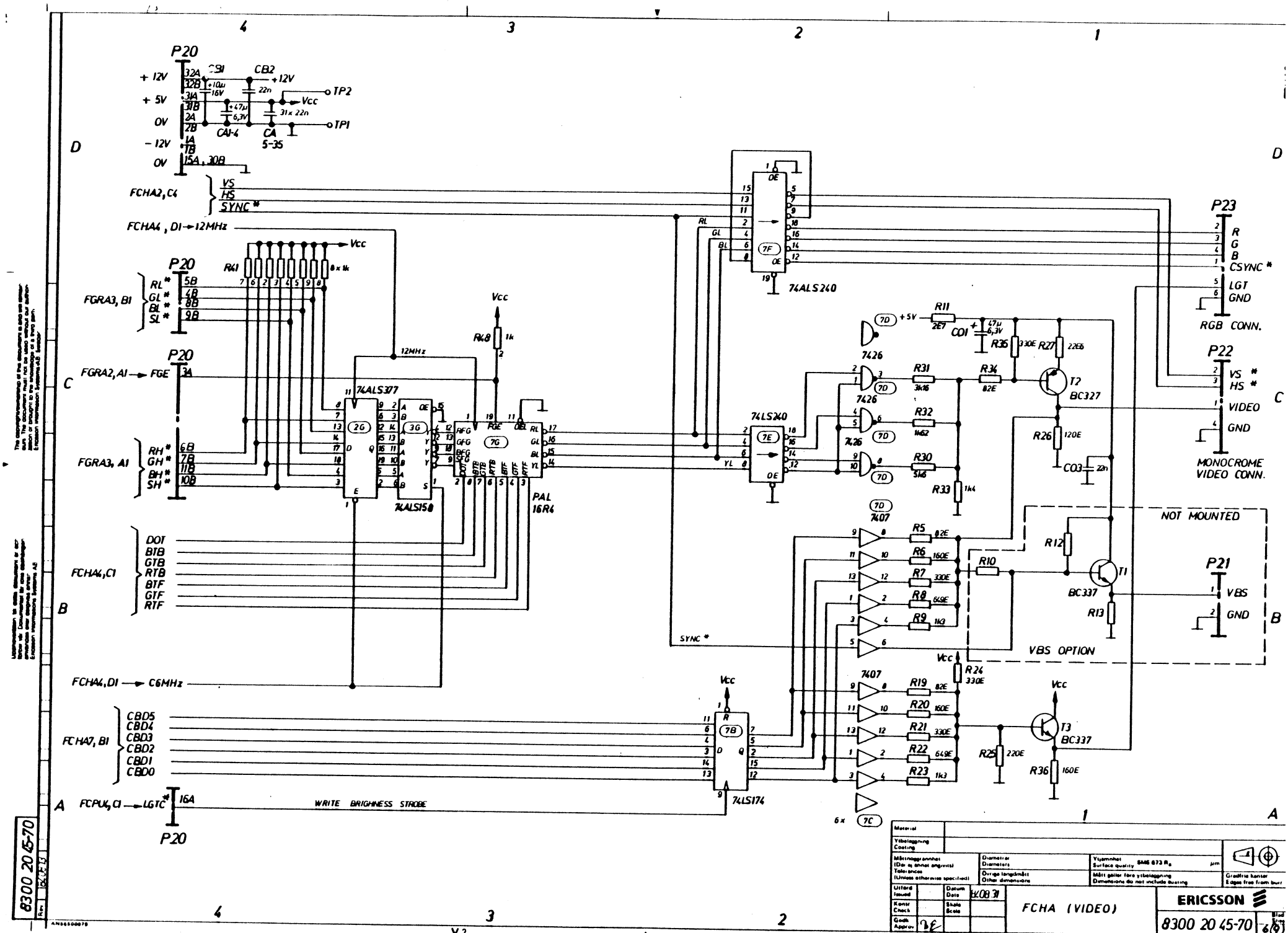


CPU BLOCK DIAGRAM
(FCPU)




P20
FCPU2,C4
6MHZ
R16
47E
74F374
6MHZ
RC=2MHZ
74ALS163
74LS240
R38
470
R37
470
C05
100p
X1
XTAL:12MHZ
C04
47p
S2
CX1 option
74ALS00A
74ALS04
12MHZ
74F02
CLKP
CLKP*
FGRA2,D4
H6MHZ
H6MHZ
R17
47E
R15
47E
74LS166A
Clear
CINH
74LS379
74F374
74LS378
C6MHZ
FCHA6,B4
12MHZ
FCHA6,D4
CCLK
CCLK*
FCHA2,C1
DOT
BTB
GTB
RTB
BTF
GTF
RTF
FCHA6,B4
RA0
RA1
RA2
RA3
FLSHCLK
FCHA2,C1
FCHA5,C1
CGD5
CGD4
CGD3
CGD2
CGD1
CGD0
CGA0
CGA1
CGA2
CGA3
FCHA5,C1
PROM:RAD
7621
4x1k
R29
CGA12
not used
CUR+4
FCHA5,B1
CGA4
CGA5
CGA6
CGA7
CGA8
CGA9
CGA10
CGA11
74LS377
74LS379
40H273
R29
1k
TEXT OFF*
TX OFF
TX OFF*
FCHA7,C4
FCHA2,B
FCHA5,C
FCHA8,D
CLKP=2MHZ
not used
TX DATA
FCHA3,D4
THP
E6P
E5P
FLP
F1P
B7P
B6P
B5P
F4P
F3P
F2P
FCHA8,D4
FCHA8,D3
FCHA8,D3
FCHA (CHAR GEN)
ERICSSON
8300 2045-70
8300 20 45-70


2 x 2Kb RAM
TC5517AP
Vcc
R29
1k
74LS368A
4040B
74ALS04
3 x 74ALS157
74ALS00A
74ALS465
81LS95
P20
FCPU2,B4
FCPU4,C1
SCG
WRITE (STROBE) SOFT CHAR. GEN
FCHA7, B1
CBD0
CBD1
CBD2
CBD3
CBD4
CBD5
CBD6
CBD7
OUT* EN
R/W
DATA IN/OUT
CHAR. DOT PATTERN
CLKP
FCHA4, A1
CGD5
CGD4
CGD3
CGD2
CGD1
CGD0
FCHA4, C4
CGA0
CGA1
CGA2
CGA3
FCHA4, B4
NO CONNECTION — CGA12
CGA4
CGA5
CGA6
CGA7
CGA8
CGA9
CGA10
CGA11
TXOFF*
FCHA4, B1
FCHA (SOFT CG)
ERICSSON
8300 20 45-70



8300 2045-70

Rev

Material
Ytbeläggning / Coating
Måttoleranser (Där ej annat anges) / Tolerances (Unless otherwise specified)
Diameter / Diameters
Övriga längdmått / Other dimensions
Ytjämnhet / Surface quality 6446 673 R_a µm
Mått gäller före ytbeläggning / Dimensions do not include coating
Gradfria kanter / Edges free from burr

Utförd / Issued — Datum / Date 94 08 31
Kontr / Check — Skala / Scale
Godk / Approv

FCHA (VIDEO)

ERICSSON

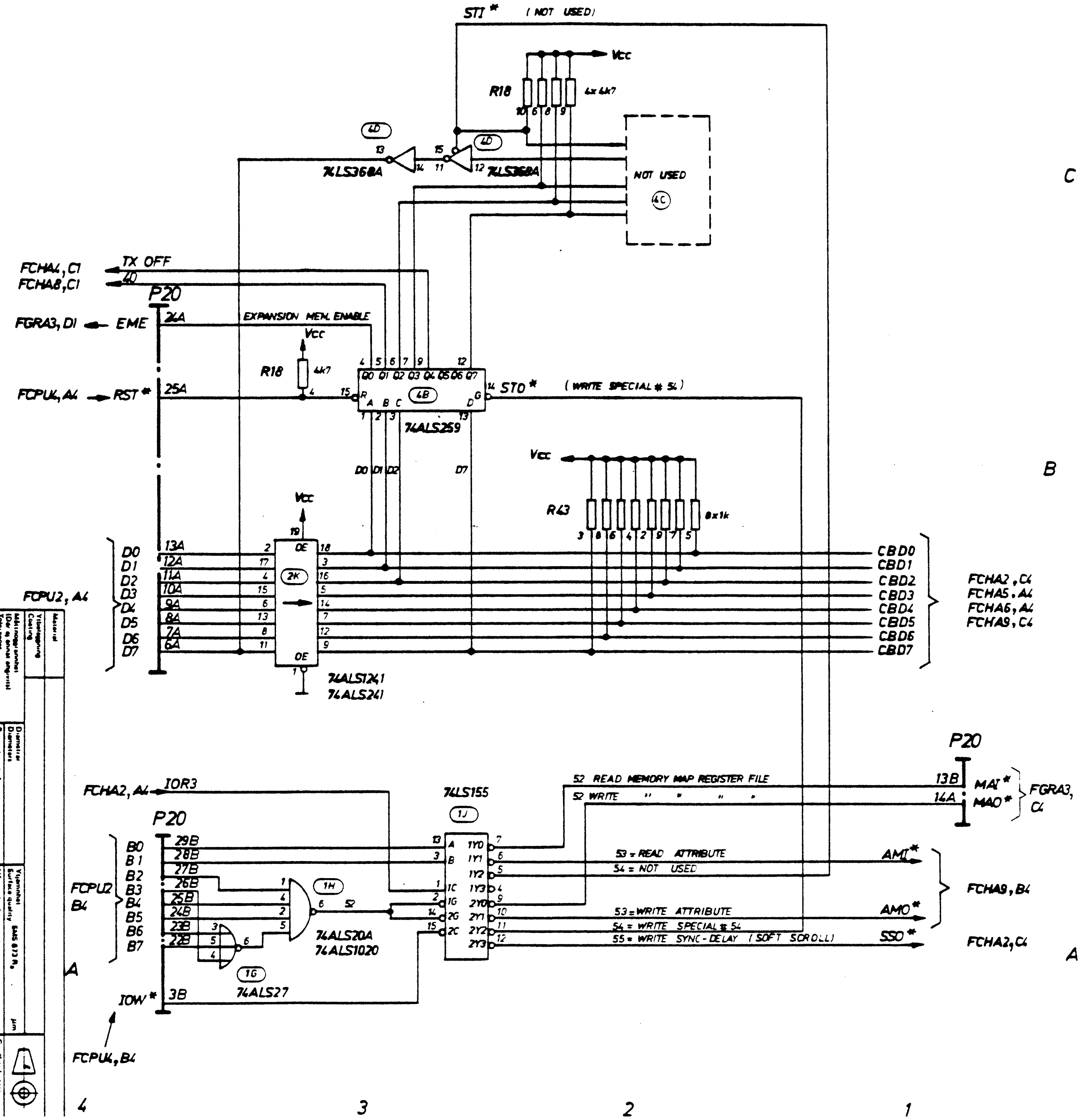
8300 20 45-70

Blad / Sheet 6 (6)

8300 20 45-70

				B	7	6	5	4	3	2	1	0	
INP/OUT	52	READ/WRITE MEMORY MAP REGISTER FILE			0	0	1	1	0	1	0	0	= 52
INP/OUT	53	READ/WRITE ATTRIBUTE			0	0	1	1	0	1	0	1	= 53
OUT	54	WRITE SPECIAL # 54			0	0	1	1	0	1	1	0	= 54
OUT	55	WRITE SYNC DELAY (SOFT SCROLL)			0	0	1	1	0	1	1	1	= 55

			128	64	32	16	8	4	2	1	
WRITE SPECIAL OUT 54,DATA		D	7	6	5	4	3	2	1	0	SIGNAL
128	ENABLE MEMORY MAPPER (SYSTEM USE ONLY)		1	0	0	0	0	0	0	0	EME
0	DISABLE MEMORY MAPPER (SYSTEM USE ONLY)		0	0	0	0	0	0	0	0	$\overline{EME}$
129	WIDTH 40 BASIC STATEMENT		1	0	0	0	0	0	0	1	40
1	WIDTH 80 BASIC STATEMENT		0	0	0	0	0	0	0	1	$\overline{40}$
132	TEXT OFF → ENABLE WRITE TO CHARACTER GEN.		1	0	0	0	0	1	0	0	TX OFF
4	TEXT → DO NOT WRITE TO CHARACTER GEN.		0	0	0	0	0	1	0	0	$\overline{TX\ OFF}$

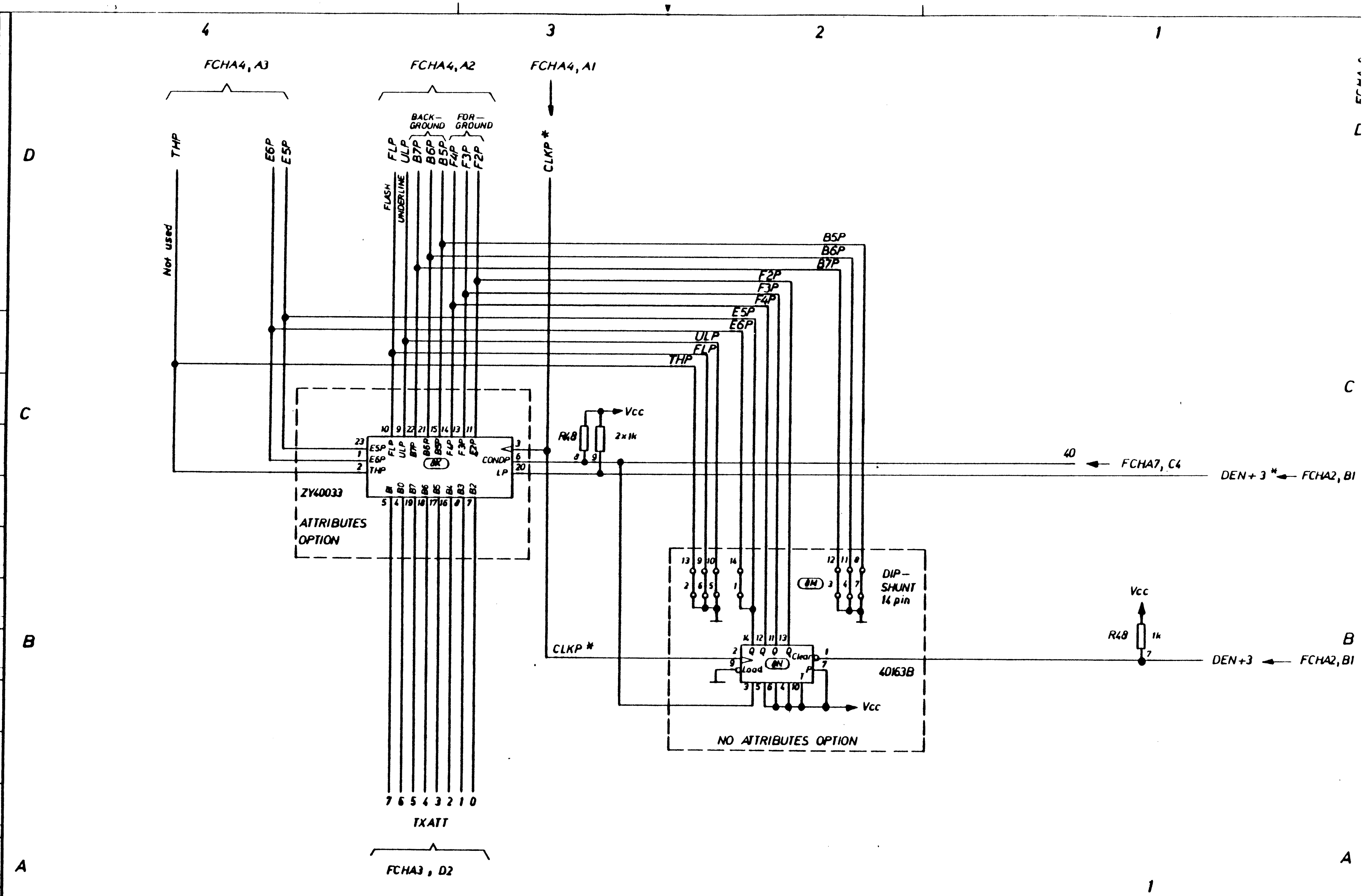


STI * (NOT USED)
Vcc
R18 4x4k7
74LS368A
NOT USED
4C
FCHA4, C1
FCHA8, C1
TX OFF
40
P20
FGRA3, D1 EME
24A
EXPANSION MEM. ENABLE
R18 4k7
FCPU4, A4 RST *
25A
74ALS259
STO * (WRITE SPECIAL # 54)
R43 8x1k
74ALS1241
74ALS241
D0 D1 D2 D3 D4 D5 D6 D7
FCPU2, A4
CBD0 CBD1 CBD2 CBD3 CBD4 CBD5 CBD6 CBD7
FCHA2, C4
FCHA5, A4
FCHA6, A4
FCHA9, C4
FCHA2, A4 IOR3
74LS155
52 READ MEMORY MAP REGISTER FILE
52 WRITE " " " "
13B MA1 *
14A MA0 *
FGRA3, C4
B0 B1 B2 B3 B4 B5 B6 B7
FCPU2 B4
74ALS20A
74ALS1020
74ALS27
53 = READ ATTRIBUTE
54 = NOT USED
53 = WRITE ATTRIBUTE
54 = WRITE SPECIAL # 54
55 = WRITE SYNC-DELAY (SOFT SCROLL)
AM1 *
AM0 *
SSO *
FCHA9, B4
FCHA2, C4
IOW * 3B
FCPU4, B4

FCHA (IOSTB)

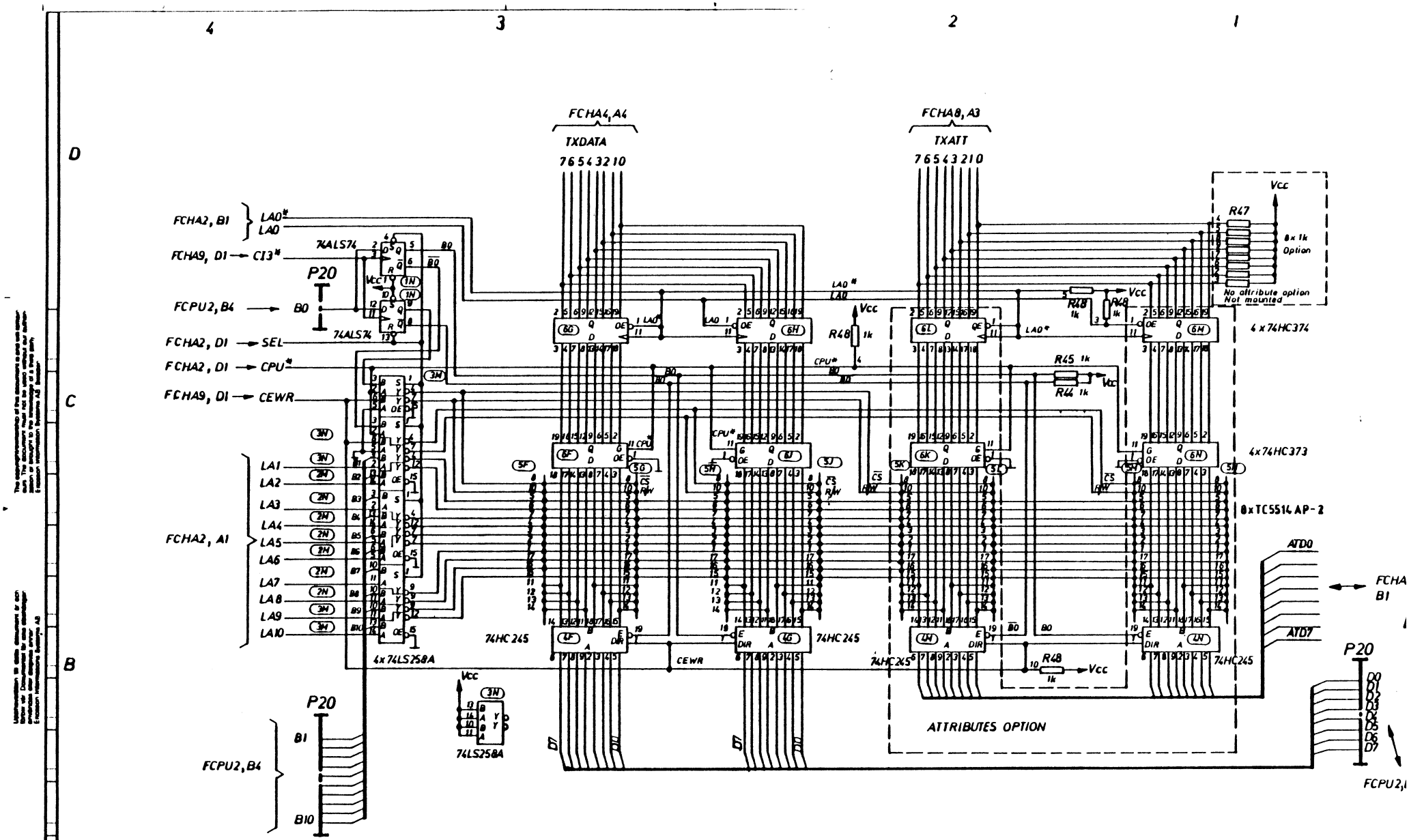
8300 2045-70

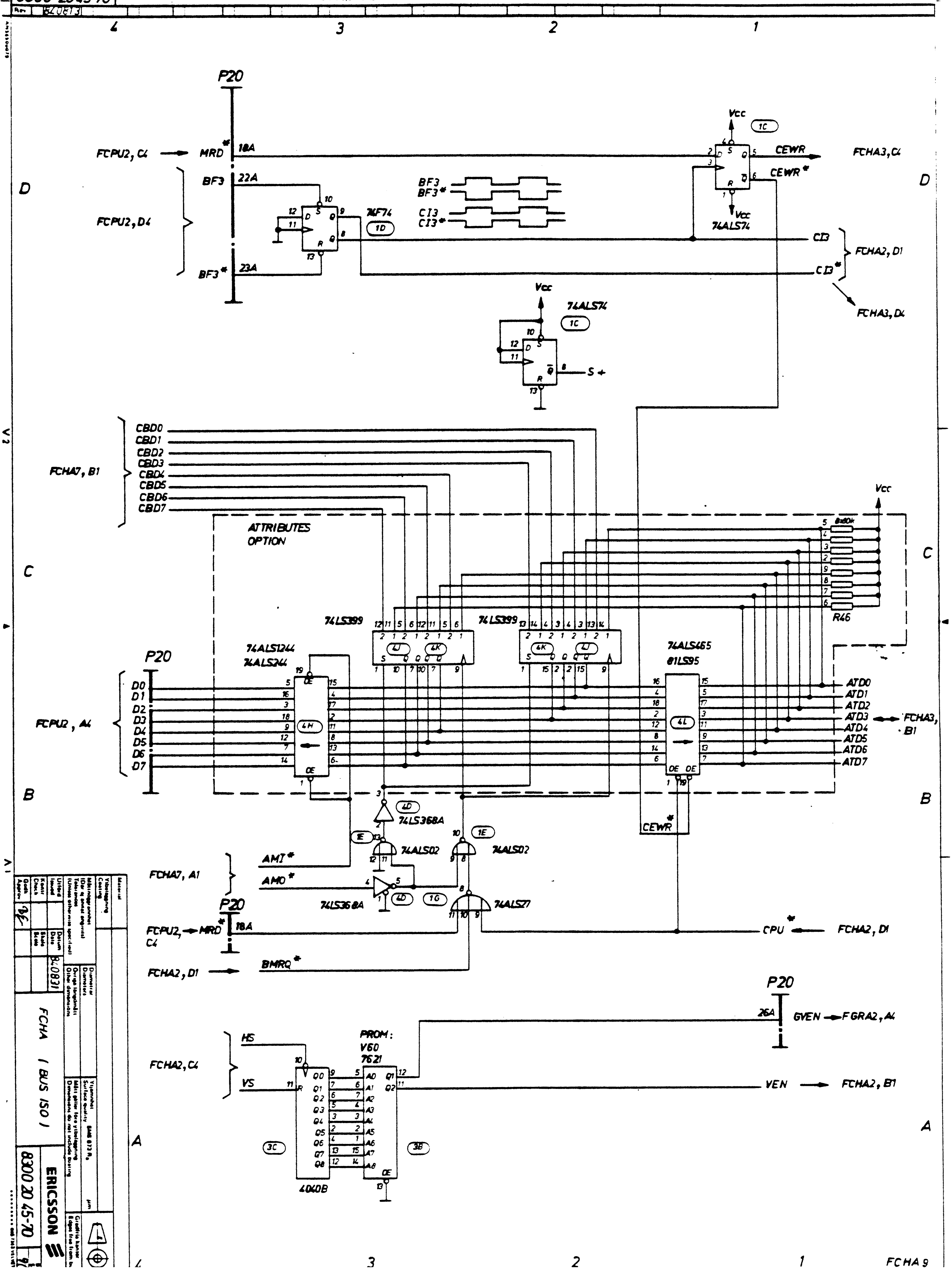
ERICSSON



Utfärd Issued	Datum Date 840831	FCHA (ATTHAND)	ERICSSON
Kontr Check	Skala Scale		8300 20 45-70

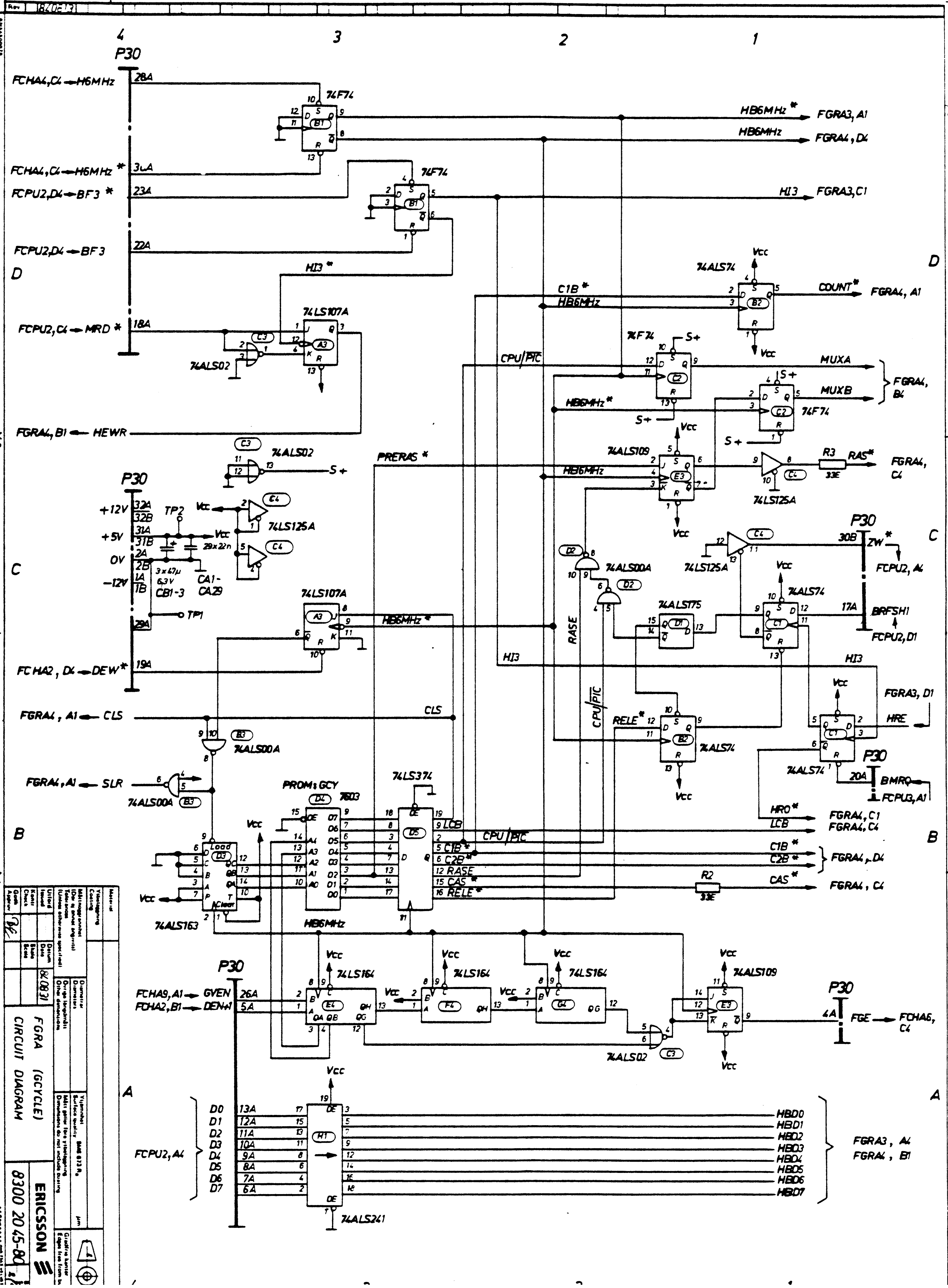
8300 20 45-70

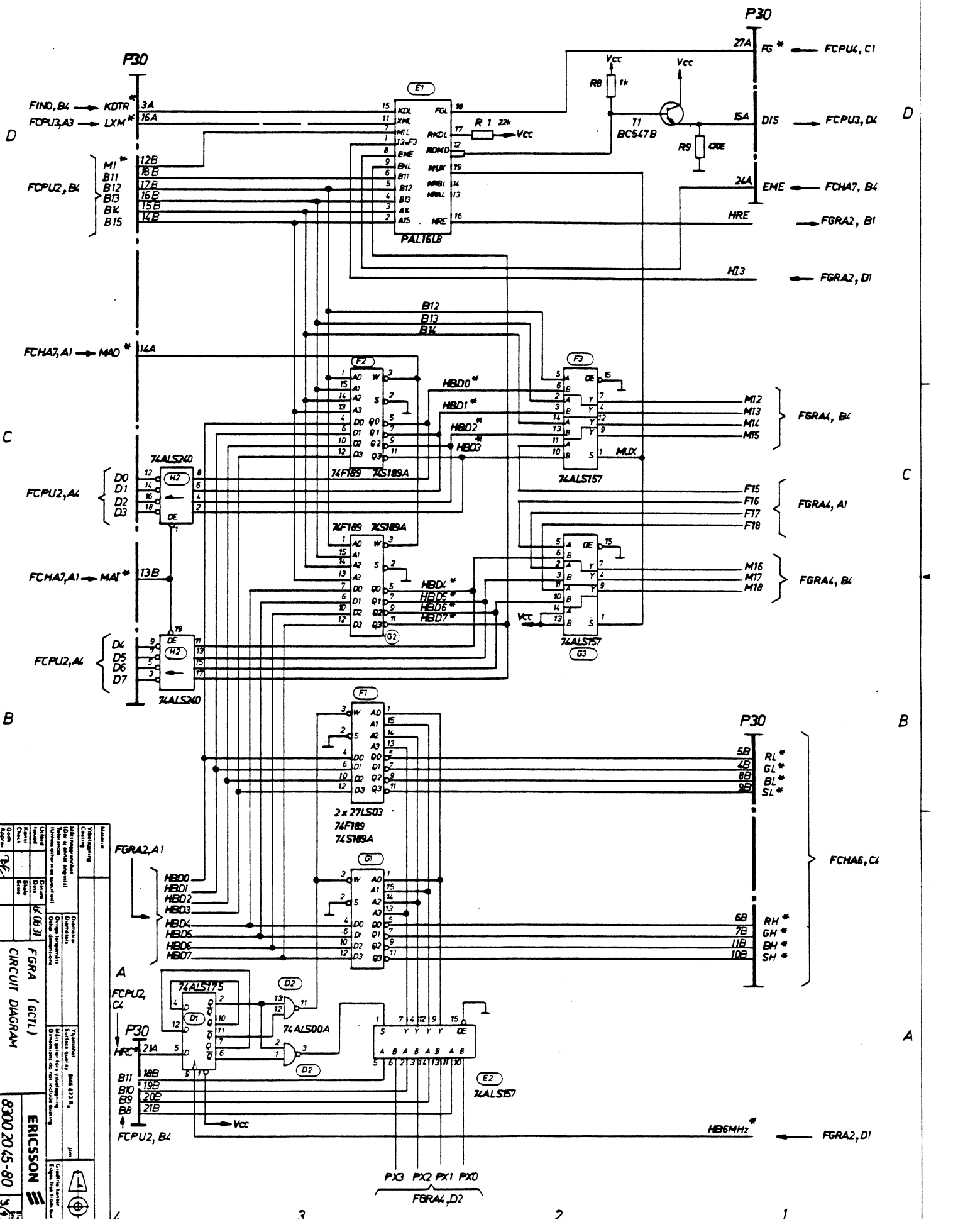

FCHA4, A4
TXDATA
7 6 5 4 3 2 1 0
FCHA8, A3
TXATT
7 6 5 4 3 2 1 0
FCHA2, B1
LA0*
LA0
FCHA9, D1 → CI3*
FCPU2, B4 → B0
FCHA2, D1 → SEL
FCHA2, D1 → CPU*
FCHA9, D1 → CEWR
FCHA2, A1
LA1
LA2
LA3
LA4
LA5
LA6
LA7
LA8
LA9
LA10
74ALS74
P20
74ALS74
4x74LS258A
74HC245
74HC245
74HC245
74HC245
74LS258A
CEWR
Vcc
R47
8x 1k
Option
No attribute option
Not mounted
R48 1k
R45 1k
R44 1k
4x74HC374
4x74HC373
8xTC5514AP-2
ATTRIBUTES OPTION
AD0
AD7
FCHA
B1
P20
FCPU2, B4
B1
B10
D0
D1
D2
D3
D4
D5
D6
D7
FCPU2,
8300 2045-70
FCHA (CHAR MEM)
ERICSSON
8300 2045-70


P20
FCPU2, C4
MRD*
18A
BF3
22A
FCPU2, D4
BF3*
23A
74F74
1D
BF3
BF3*
CI3
CI3*
Vcc
1C
CEWR
CEWR*
FCHA3, C4
74ALS74
CI3
CI3*
FCHA2, D1
FCHA3, D4
74ALS74
S+
CBD0
CBD1
CBD2
CBD3
CBD4
CBD5
CBD6
CBD7
FCHA7, B1
ATTRIBUTES OPTION
74LS399
74LS399
74ALS465
81LS95
R46
74ALS1244
74ALS244
FCPU2, A4
ATD0
ATD1
ATD2
ATD3
ATD4
ATD5
ATD6
ATD7
FCHA3, B1
74LS368A
74ALS02
74ALS02
74ALS27
CEWR*
FCHA7, A1
AM1*
AM0*
74LS368A
FCPU2, C4
MRD*
FCHA2, D1
BMRQ*
CPU*
FCHA2, D1
P20
26A
GVEN
FGRA2, A4
FCHA2, C4
HS
VS
PROM:
V60
7621
VEN
FCHA2, B1
4040B

ERICSSON
FCHA I BUS ISO I
8300 20 45-70

8300 20 45-80

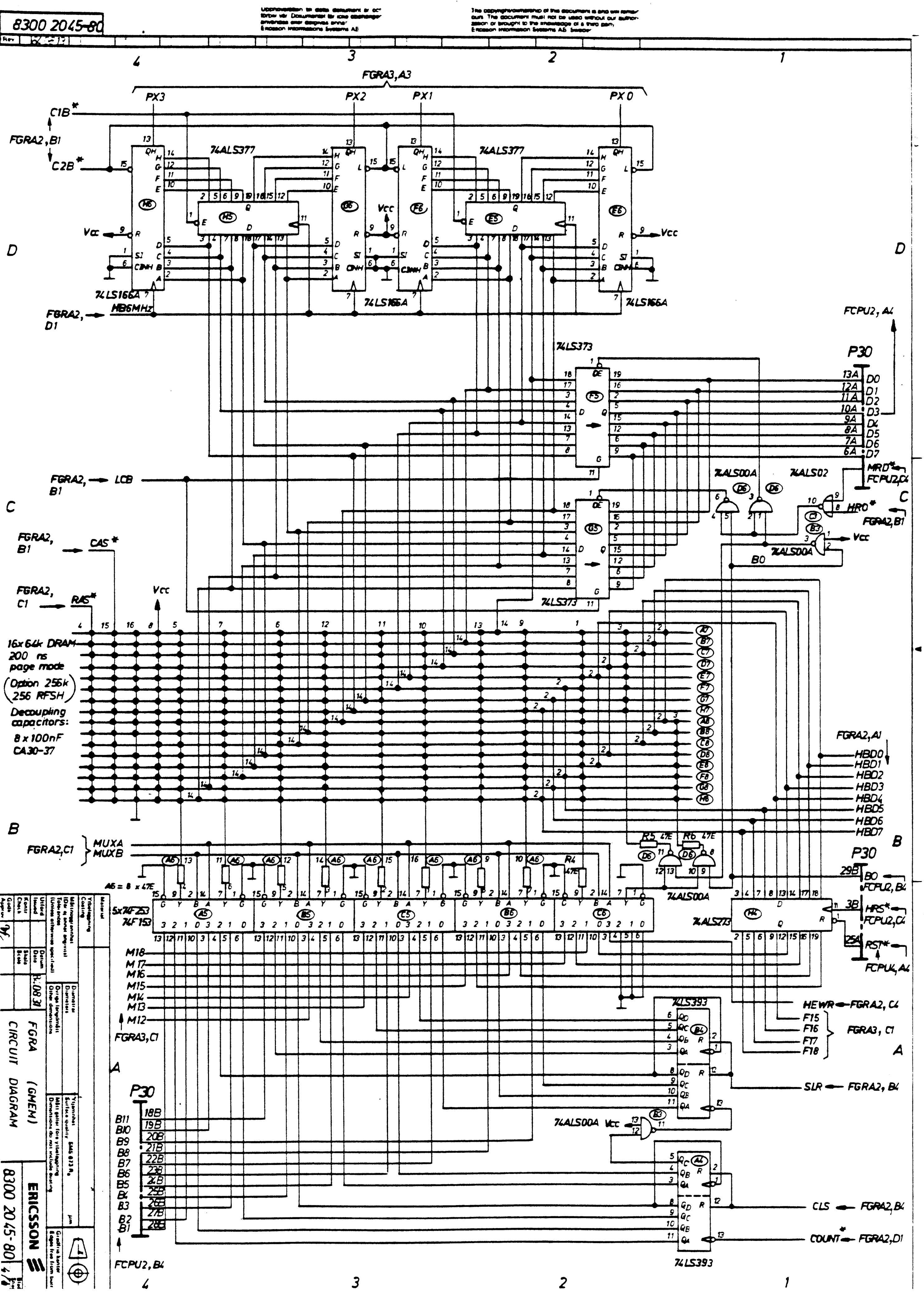

P30
FCHA4,C4 ← H6MHz
FCHA4,C4 ← H6MHz *
FCPU2,D4 ← BF3 *
FCPU2,D4 ← BF3
FCPU2,C4 ← MRD *
FGRA4,B1 ← HEWR
FCHA2, D4 ← DEW *
FGRA4, A1 ← CLS
FGRA4,A1 ← SLR
74F74
74LS107A
74ALS02
74ALS74
74ALS109
74LS125A
74ALS00A
74ALS175
74ALS163
PROM: GCY
74LS374
74LS164
74ALS241
HB6MHz * → FGRA3, A1
HB6MHz → FGRA4, D4
HI3 → FGRA3,C1
COUNT * → FGRA4, A1
MUXA
MUXB
FGRA4, B4
RAS * → FGRA4, C4
ZW * → FCPU2, A4
BRFSH1 → FCPU2,D1
FGRA3, D1
HRE
BMRQ ← FCPU3,A1
HRO * → FGRA4,C1
LCB → FGRA4,C4
C1B *
C2B * → FGRA4, D4
CAS * → FGRA4, C4
FGE → FCHA6, C4
FCHA9,A1 ← GVEN
FCHA2,B1 ← DEN+1
PRERAS *
CPU/PIC
RASE
RELE *
R2 33E
R3 33E
+12V
+5V
0V
-12V
TP1
TP2
3 x 47µ 6,3V CB1-3
29x22n
CA1-CA29
FCPU2,A4
D0 D1 D2 D3 D4 D5 D6 D7
HBD0 HBD1 HBD2 HBD3 HBD4 HBD5 HBD6 HBD7
FGRA3, A4
FGRA4, B1
FGRA (GCYCLE)
CIRCUIT DIAGRAM
8300 2045-80
ERICSSON



FGRA (GCTL) CIRCUIT DIAGRAM

8300 2045-80

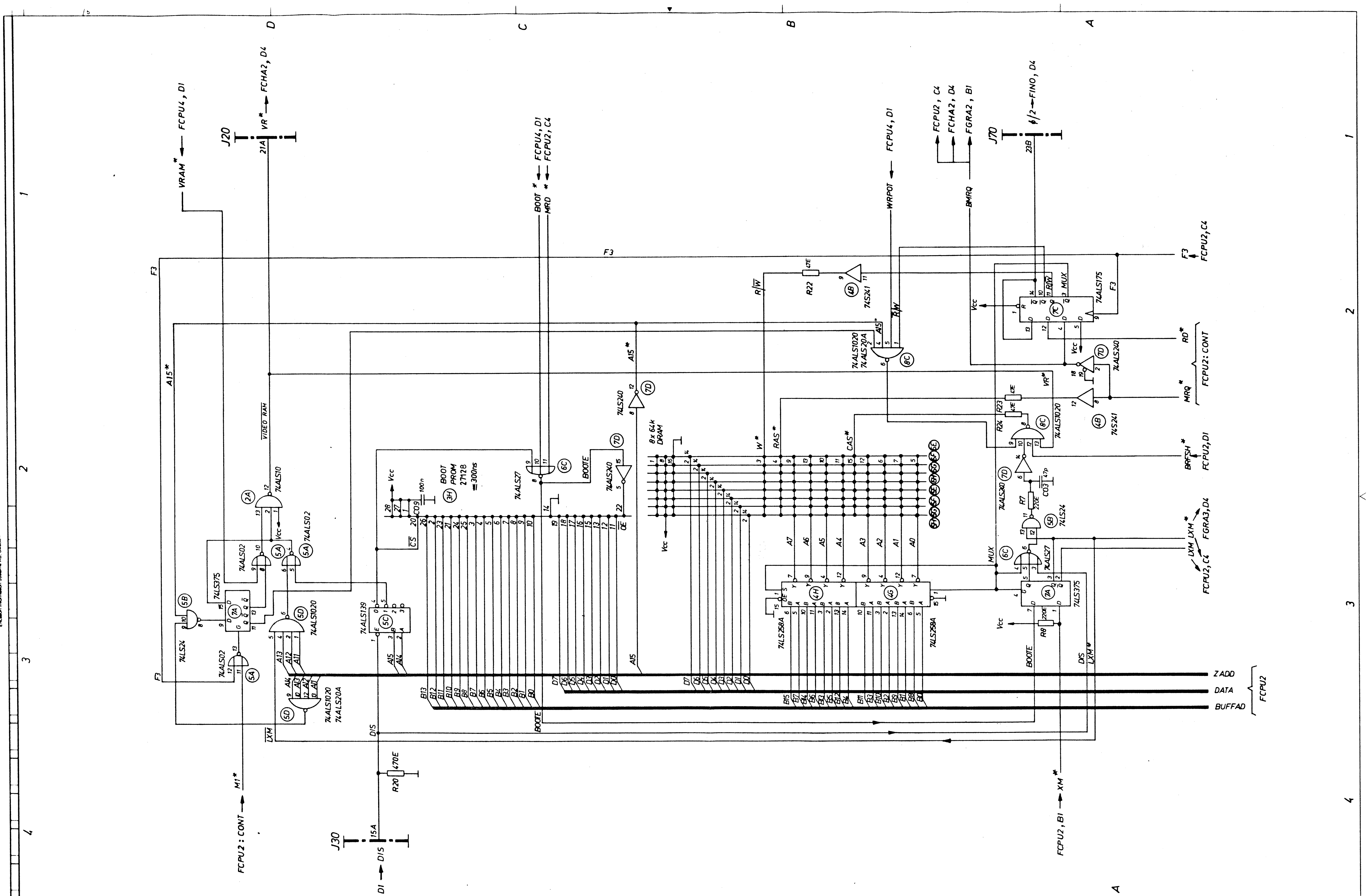
ERICSSON



8300 2045-80
FGRA3,A3
PX3
PX2
PX1
PX0
C1B*
FGRA2,B1
C2B*
74ALS377
74LS166A
HB6MHz
FGRA2, D1
74LS373
P30
D0
D1
D2
D3
D4
D5
D6
D7
FCPU2,A4
MRD*
FCPU2,C4
74ALS00A
74ALS02
HRO*
FGRA2,B1
FGRA2, B1 LCB
FGRA2, B1 CAS*
FGRA2, C1 RAS*
Vcc
16x64k DRAM 200 ns page mode
(Option 256k 256 RFSH)
Decoupling capacitors: 8x100nF CA30-37
FGRA2,A1
HBD0
HBD1
HBD2
HBD3
HBD4
HBD5
HBD6
HBD7
FGRA2,C1 MUXA MUXB
A6 = 8 x 47E
R4 47E
R5 47E
R6 47E
5x74F253 74F153
74ALS273
BO
FCPU2,B4
HRS*
FCPU2,C4
RST*
FCPU4,A4
M18
M17
M16
M15
M14
M13
M12
FGRA3,C1
74LS393
HEWR FGRA2, C4
F15
F16
F17
F18
FGRA3, C1
SLR FGRA2, B4
74ALS00A
B11
B10
B9
B8
B7
B6
B5
B4
B3
B2
B1
FCPU2, B4
CLS FGRA2,B4
COUNT* FGRA2,D1
FGRA (GMEM)
CIRCUIT DIAGRAM
8300 2045-80
ERICSSON

FCPU (CPU) CIRCUIT DIAGRAM

8300 2045-60



Datum / Date: 840831

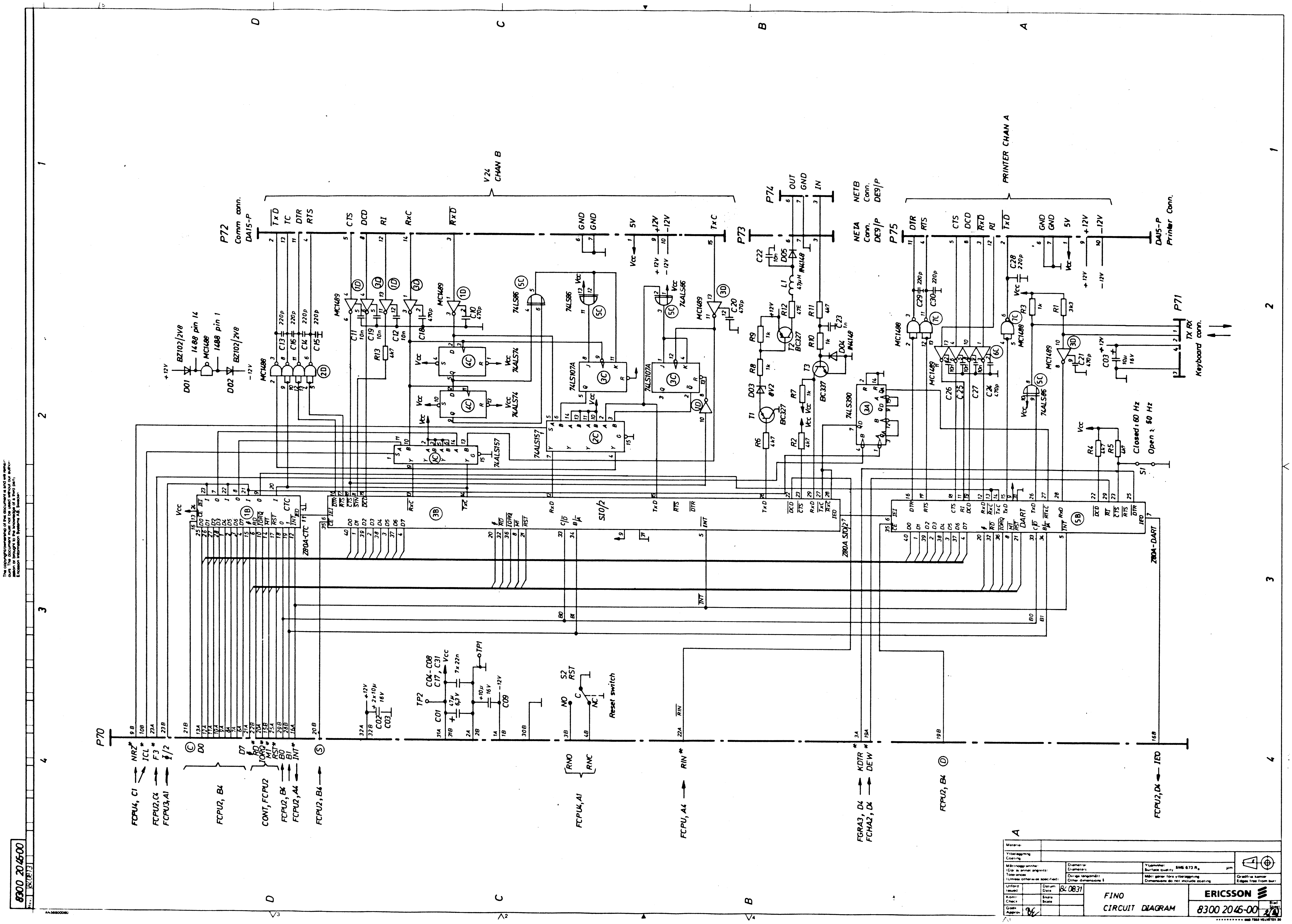
FCPU (MEM)

CIRCUIT DIAGRAM

ERICSSON

8300 20 45-60

Blad / Sheet: 3 (4)



V24 CHAN B
PRINTER CHAN A
P72 Comm conn. DA15-P
P73
P74
P75
NETA Conn. DE9/P
NETB Conn. DE9/P
P71 Keyboard conn.
DA15-P Printer Conn.
P70
Z80A-CTC
Z80A SIO/2
Z80A-DART
Reset switch
Closed: 60 Hz
Open: 50 Hz
FINO
CIRCUIT DIAGRAM
ERICSSON
8300 2046-00

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8300 20 45-60

FCPU (RCLOCK)

CIRCUIT DIAGRAM

8300 20 45-60

ERICSSON

Ericsson Information Systems AB
Sektor Arbetsplatser/Sector Workstations
S-205 25 MALMÖ SWEDEN