

IC-KRETSAR ABC 80

Typ		Sp.matn.	Pinnar	Pos	Sid
74LS04	Sex inverterare	5 V	14	E6	1
04	" "	5 V	14	H8	
06	Buffer/Driver	5 V	14	H7	1
LS08	Fyra 2-ing. and -grindar	5 V	14	E3, H5, K7	1
LS10	Tre 3-ing. N and -grindar	5 V	14	E5, G3	1
LS32	Fyra 2-ing. or -grindar	5 V	14	H3, H4, F8	2
LS74A	Två D-vippor	5 V	14	G5	2
74	" "	5 V	14	F6	
LS86	Fyra 2-ing. X or -grindar	5 V	14	G6	3
LS107	Två J-K vippor	5 V	14	B5, G4, J5	3
LS132	Fyra 2-ing. N and -Schmitt trigger	5 V	14	F7	4
LS139	Två "en av fyra" avkodare	5 V	16	E4	5
LS145	BCD-decimal avkodare	5 V	16	J2	6
LS161A	Synkron 4-bit räknare	5 V	16	H6	7
LS166	8-bit skiftregister	5 V	16	J1, J6	8
LS175	Fyra D-vippor, gemensam clock & clear	5 V	16	J4	9
LS241	8-bit buffert	5 V	20	D8, C8	10
LS245	Dubbelriktad 8-bit buffert	5 V	20	F1, B8	10
LS257	4-bit multiplexer	5 V	16	B2, B3, B4, E1, E2, F5	11
LS 273	Åtta D-vippor, gemensam clock & clear	5 V	20	G7, H1	12
S263	Tecken - ROM	5 V	20	H2	12
LS283	4-bit heladderare	5 V	16	F3	13
LS375	4-bit latch	5 V	16	G1, G2	14
LS393	Två 4-bit binär räknare	5 V	14	F2, F4, K3, K4, K6	14
75188	Fyra linjedrivare	± 9 V	14	B9	15
75189	Fyra linjemottagare	5 V	14	A9	15
LM339	Fyra spänningskomp.	5 V	14	J8	16
8205	"En av åtta" avkodare	5 V	16	E8, E9	16
76477N	Ljudgenerator	5 V	28	G8	17
TMS4045	Ram	5 V	18	D1, C1	17
TMS4732	ROM	5 V	24	A5, A2, A3	18
TMS4116	Ram	+5 V -5 V +12V	16	C2-C5, D2-D5	18
7611	PROM	5	16	E7	19
7621	PROM	5	16	K1, K2	19
Z80 A	CPU	5	40		20
Z80	PIO	5	40		21

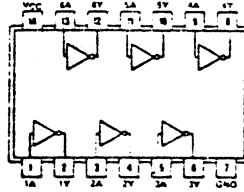
LS 04

HEX INVERTERS

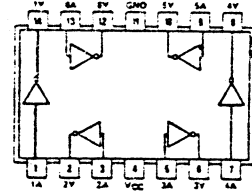
04

positive logic:
 $Y = \bar{A}$

See page 6-2



SN5404 (J) SN7404 (J, N)
 SN54H04 (J) SN74H04 (J, N)
 SN54L04 (J) SN74L04 (J, N)
 SN54LS04 (J, W) SN74LS04 (J, N)
 SN54S04 (J, W) SN74S04 (J, N)



SN5404 (W)
 SN54H04 (W)
 SN54L04 (T)

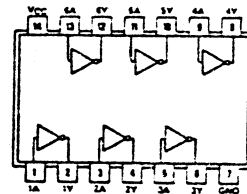
LS 06

HEX INVERTER BUFFERS/DRIVERS
 WITH OPEN-COLLECTOR
 HIGH-VOLTAGE OUTPUTS

06

positive logic:
 $Y = \bar{A}$

See page 6-24



SN5406 (J, W) SN7406 (J, N)

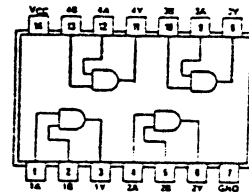
LS 08

QUADRUPLE 2-INPUT
 POSITIVE-AND GATES

08

positive logic:
 $Y = AB$

See page 6-10



SN5408 (J, W) SN7408 (J, N)
 SN54L08 (J, W) SN74L08 (J, N)
 SN54S08 (J, W) SN74S08 (J, N)

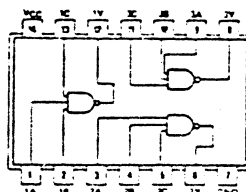
LS 10

TRIPLE 3-INPUT
 POSITIVE-NAND GATES

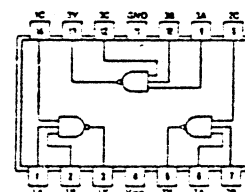
10

positive logic:
 $Y = \overline{ABC}$

See page 6-2



SN5410 (J) SN7410 (J, N)
 SN54H10 (J) SN74H10 (J, N)
 SN54L10 (J) SN74L10 (J, N)
 SN54LS10 (J, W) SN74LS10 (J, N)
 SN54S10 (J, W) SN74S10 (J, N)



SN5410 (W)
 SN54H10 (W)
 SN54L10 (T)

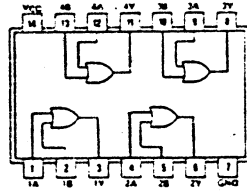
LS 32

QUADRUPLE 2-INPUT
POSITIVE-OR GATES

32

positive logic:
 $Y = A + B$

See page 6-28



SNS432 (J, W) SN7432 (J, N)
 SNS4LS32 (J, W) SN74LS32 (J, N)
 SNS4S32 (J, W) SN74S32 (J, N)

LS 74

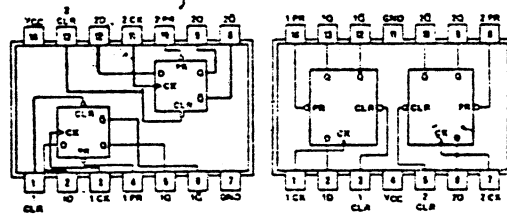
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

74

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	\bar{Q}_0

See pages 6-46, 6-50, 6-54, and 6-56



SNS474 (J) SN7474 (J, N) SNS474 (W)
 SNS4H74 (J) SN74H74 (J, N) SNS4H74 (W)
 SNS4L74 (J) SN74L74 (J, N) SNS4L74 (T)
 SNS4LS74A (J, W) SN74LS74A (J, N)
 SNS4S74 (J, W) SN74S74 (J, N)

LS 86

QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

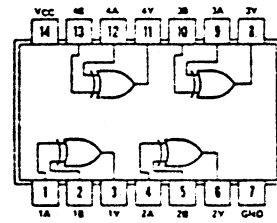
86 $Y = A \oplus B = \bar{A}B + A\bar{B}$

FUNCTION TABLE

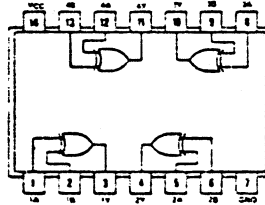
INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

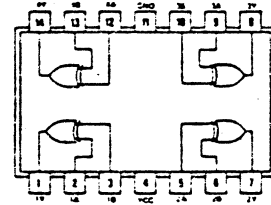
See page 7-45



SN5486 (J, W) SN7486 (J, N)
 SN54LS86 (J, W) SN74LS86 (J, N)
 SN54S86 (J, W) SN74S86 (J, N)



SN54LS86 (J) SN74LS86 (J, N)



SN54S86 (J, N)

LS 107

DUAL J-K FLIP-FLOPS WITH CLEAR

107

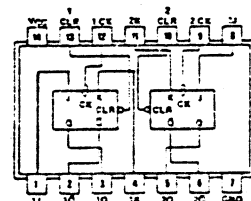
FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	\downarrow	L	L	Q_0	\bar{Q}_0
H	\downarrow	H	L	H	L
H	\downarrow	L	H	L	H
H	\downarrow	H	H	TOGGLE	TOGGLE

See pages 6-46 and 6-56

LS107A
 FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	\downarrow	L	L	Q_0	\bar{Q}_0
H	\downarrow	H	L	H	L
H	\downarrow	L	H	L	H
H	\downarrow	H	H	TOGGLE	TOGGLE
H	H	X	X	Q_0	\bar{Q}_0



SN54107 (J) SN74107 (J, N)
 SN54LS107A (J) SN74LS107A (J, N)

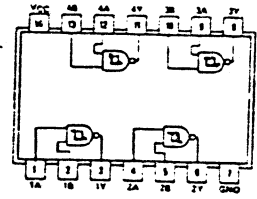
LS 132

QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

132

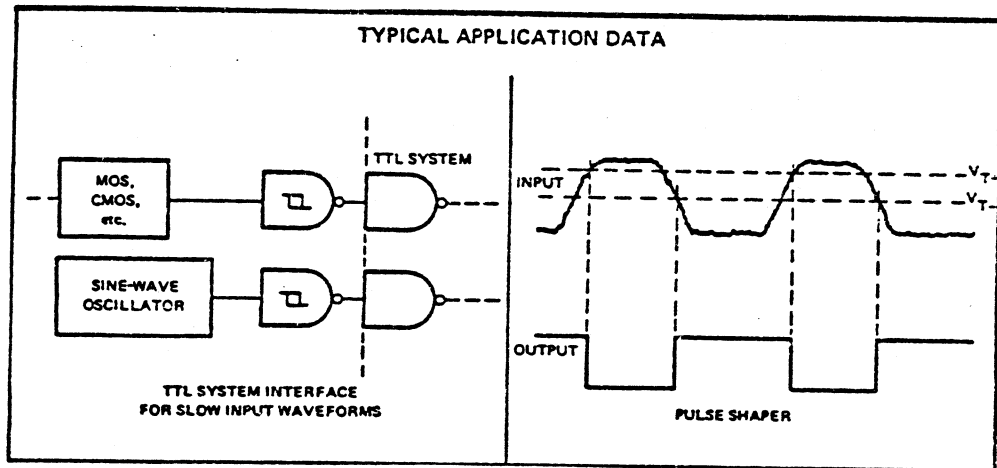
positive logic:
 $Y = \overline{AB}$

See page 8-14



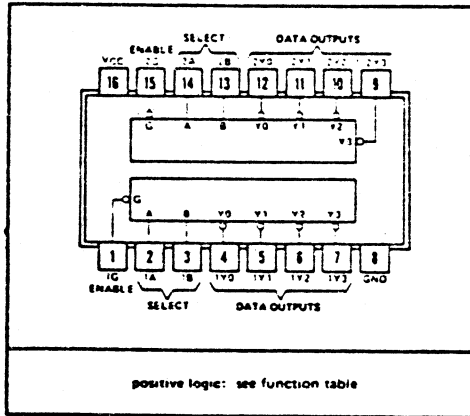
SN54132 (J, W) SN74132 (J, N)
SN54LS132 (J, W) SN74LS132 (J, N)
SN54S132 (J, W) SN74S132 (J, N)

TYPICAL APPLICATION DATA

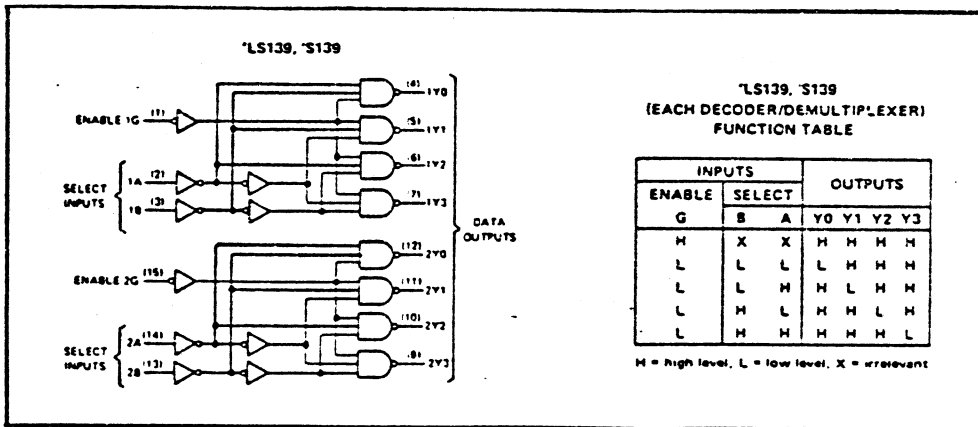


LS 139

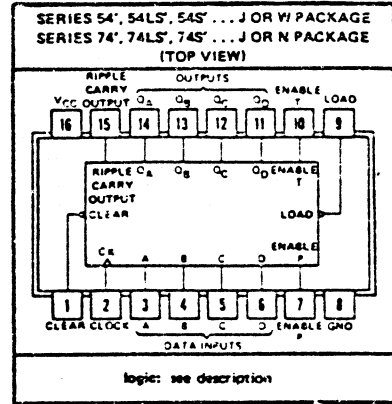
SNS4LS139, SN54S139 ... J OR W PACKAGE
 SN74LS139, SN74S139 ... J OR N PACKAGE
 (TOP VIEW)



positive logic: see function table



LS 161 A

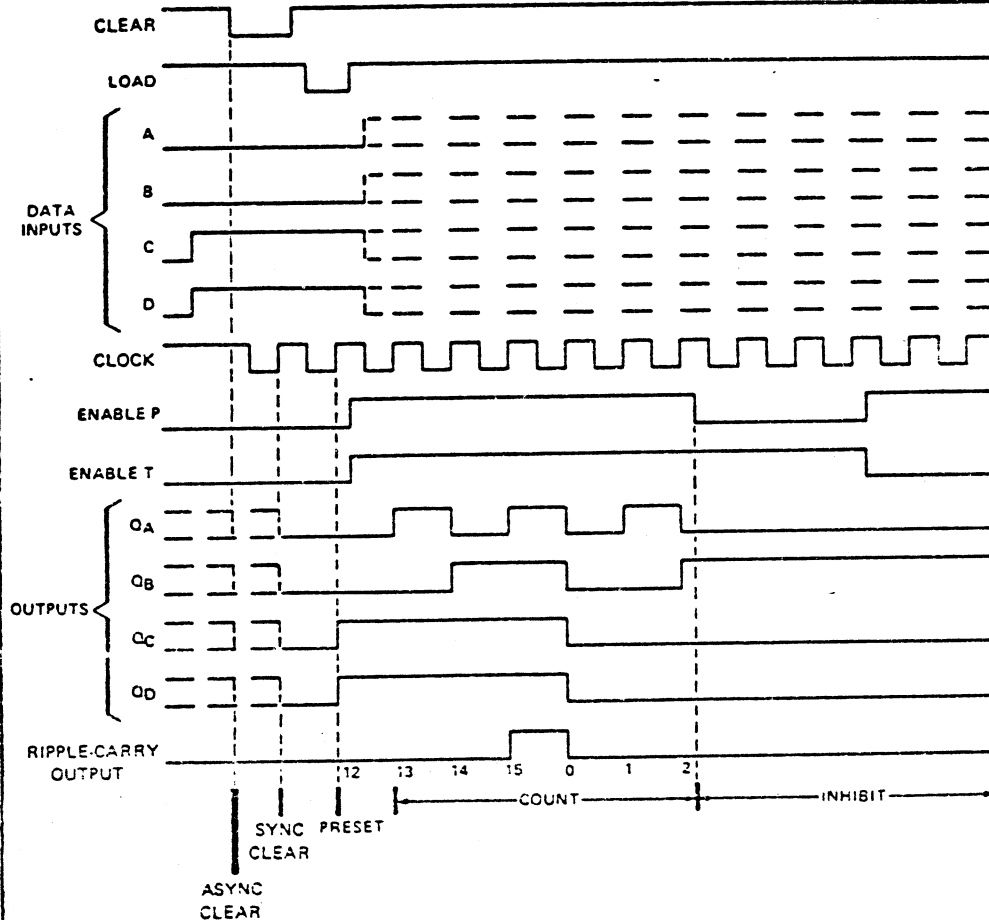


'161, 'LS161A, '163, 'LS163A, 'S163 BINARY COUNTERS

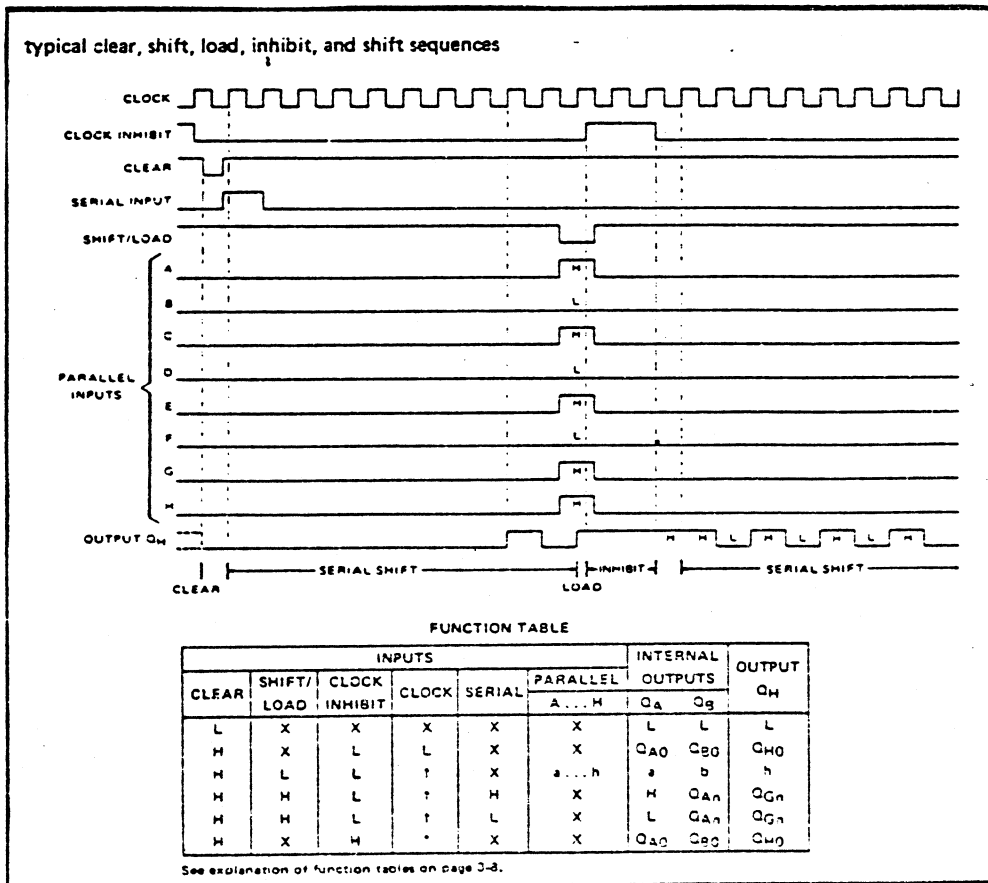
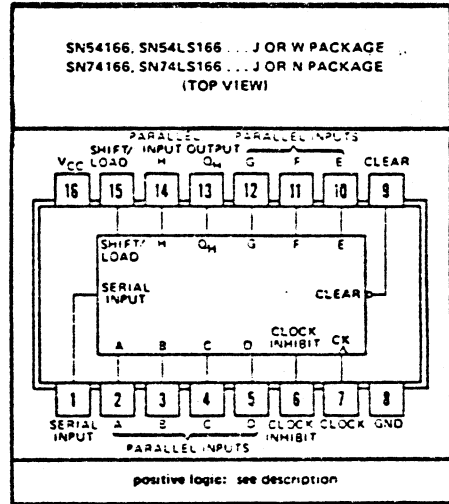
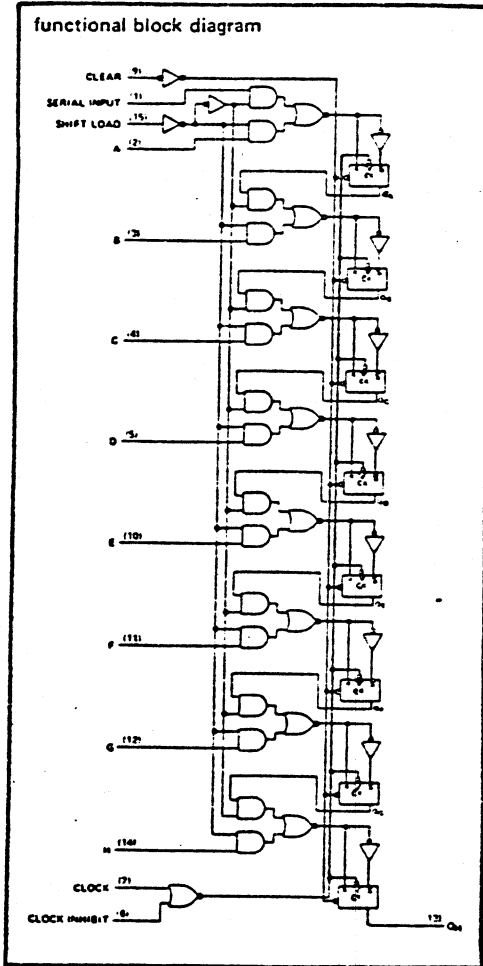
typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero ('161 and 'LS161A are asynchronous; '163, 'LS163A, and 'S163 are synchronous)
2. Preset to binary twelve
3. Count to thirteen, fourteen fifteen, zero, one, and two
4. Inhibit

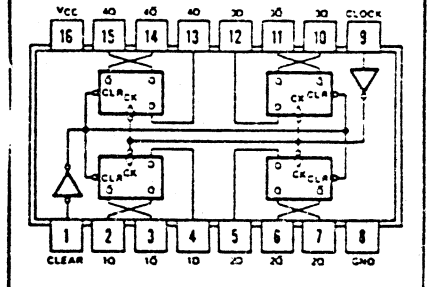


LS 166

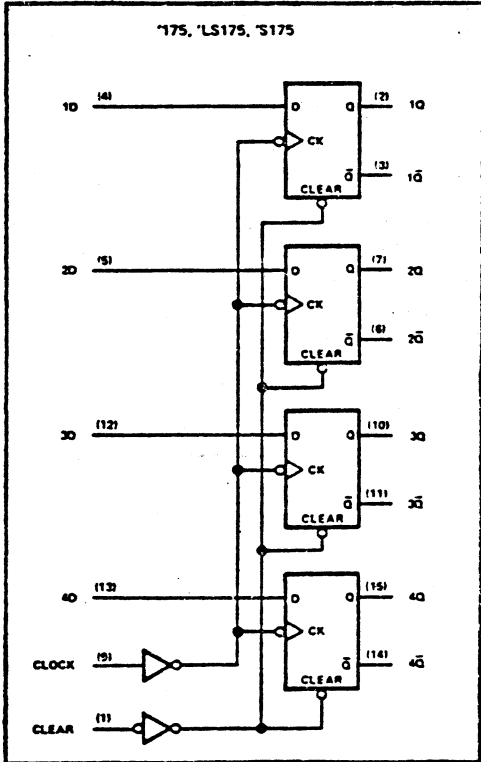


LS 175

SN54175, SN54LS175, SN54S175 . . . J OR W PACKAGE
 SN74175, SN74LS175, SN74S175 . . . J OR N PACKAGE
 (TOP VIEW)



positive logic: see function table

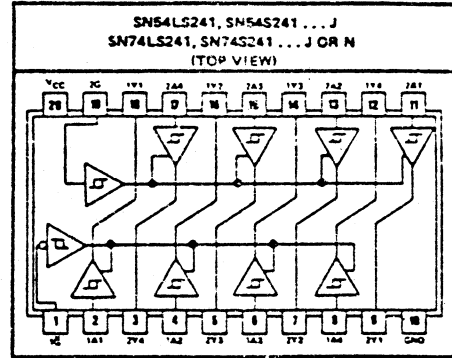


**FUNCTION TABLE
 (EACH FLIP-FLOP)**

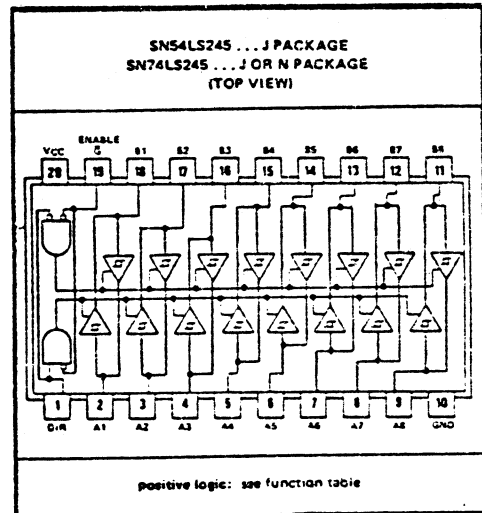
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	\bar{Q}
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	\bar{Q}_0

H = high level (steady state)
 L = low level (steady state)
 X = irrelevant
 ↑ = transition from low to high level
 Q_0 = the level of Q before the indicated steady-state input conditions were established.
 ↑ = '175, 'LS175, and 'S175-only

LS 241



LS 245



FUNCTION TABLE		
ENABLE G	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

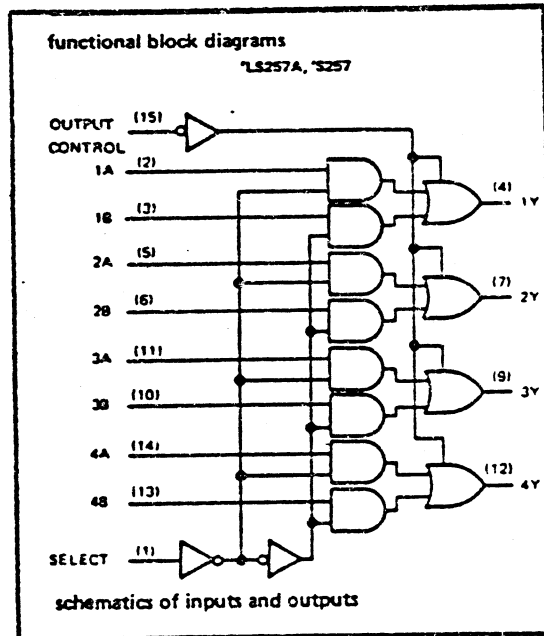
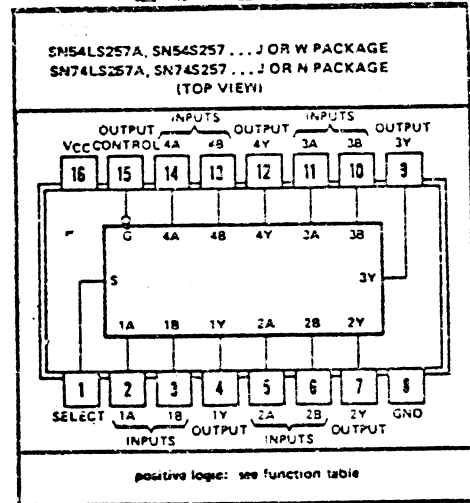
H = high level, L = low level, X = irrelevant

LS 257

FUNCTION TABLE

OUTPUT CONTROL	INPUTS			OUTPUT Y	
	SELECT	A	B	'LS257A 'S257	'LS250A 'S258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

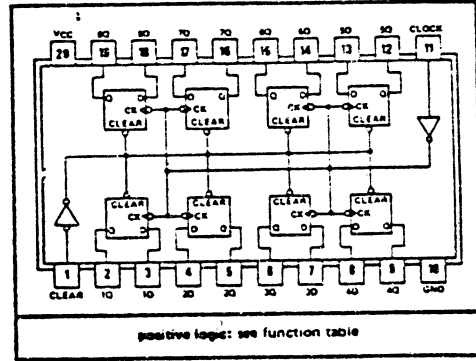


LS 273

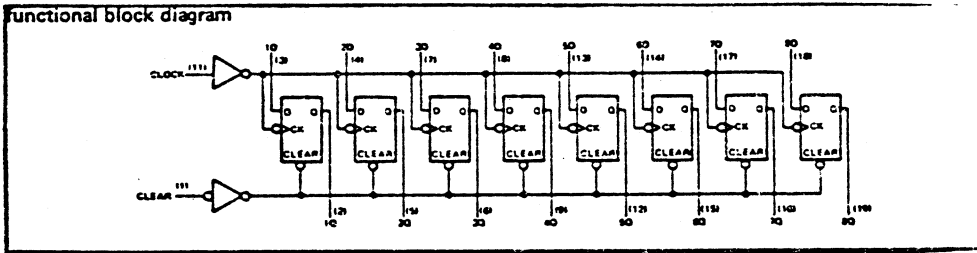
SN54273, SN54LS273 ... J PACKAGE
SN74273, SN74LS273 ... J OR N PACKAGE

FUNCTION TABLE
(EACH FLIP-FLOP)

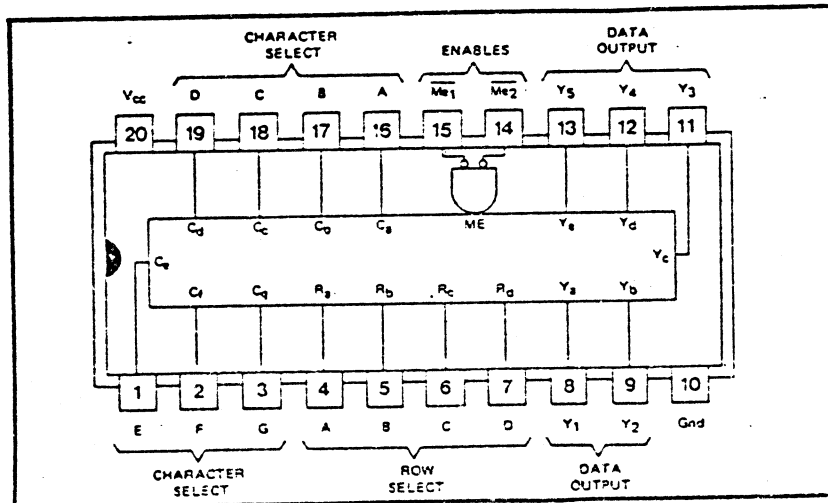
INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀



functional block diagram



S 263



LS 375

- Supply Voltage and Ground on Corner Pins To Simplify P-C Board Layout

logic

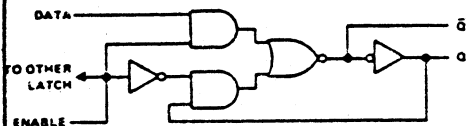
FUNCTION TABLE (EACH LATCH)

INPUTS		OUTPUTS	
D	G	Q	\bar{Q}
L	H	L	H
H	H	H	L
X	L	Q_0	\bar{Q}_0

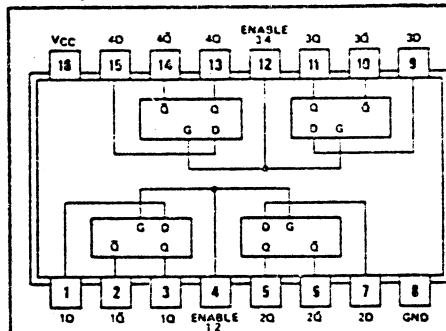
H = high level, L = low level, X = irrelevant

Q_0 = the level of Q before the high-to-low transition of G.

functional block diagram (each latch)



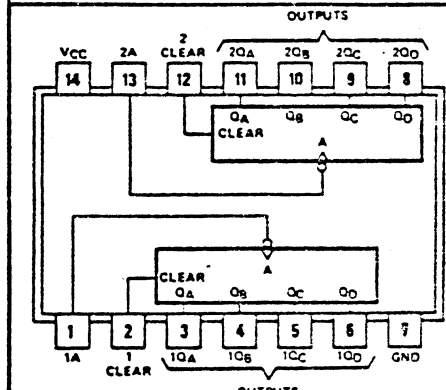
SN54LS375 ... J OR W PACKAGE
SN74LS375 ... J OR N PACKAGE
(TOP VIEW)



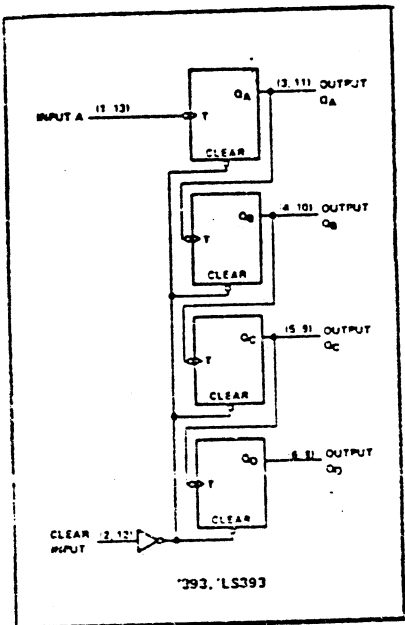
logic: see function table

LS 393

SN54393, SN54LS393 ... J OR W PACKAGE
SN74393, SN74LS393 ... J OR N PACKAGE
(TOP VIEW)



positive logic: High input to clear resets all four outputs low



"393, 'LS393
COUNT SEQUENCE
(EACH COUNTER)

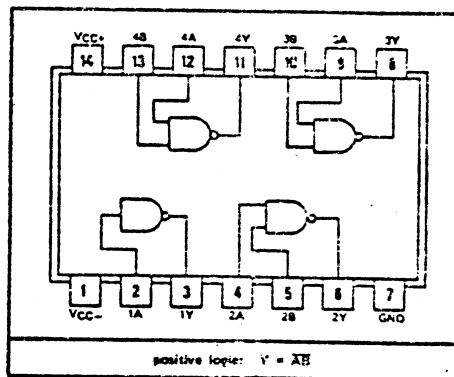
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

LS75188

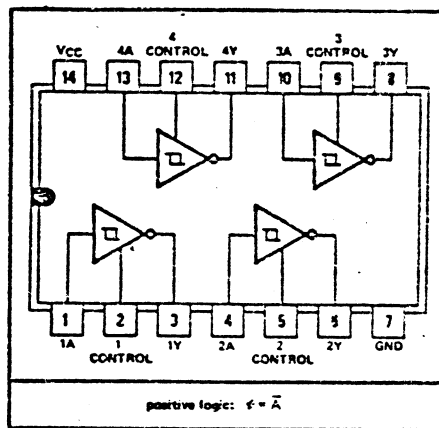
FUNCTION TABLE

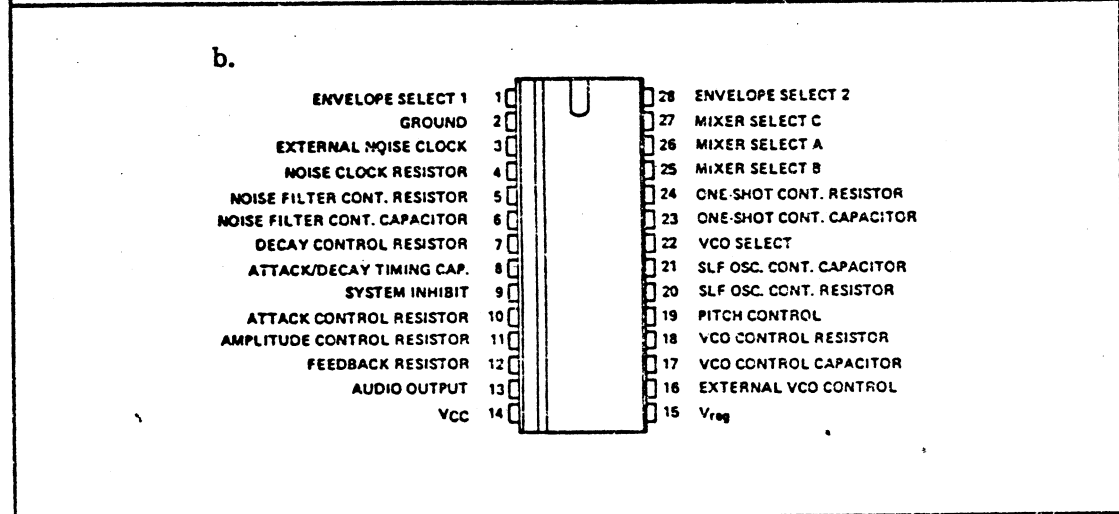
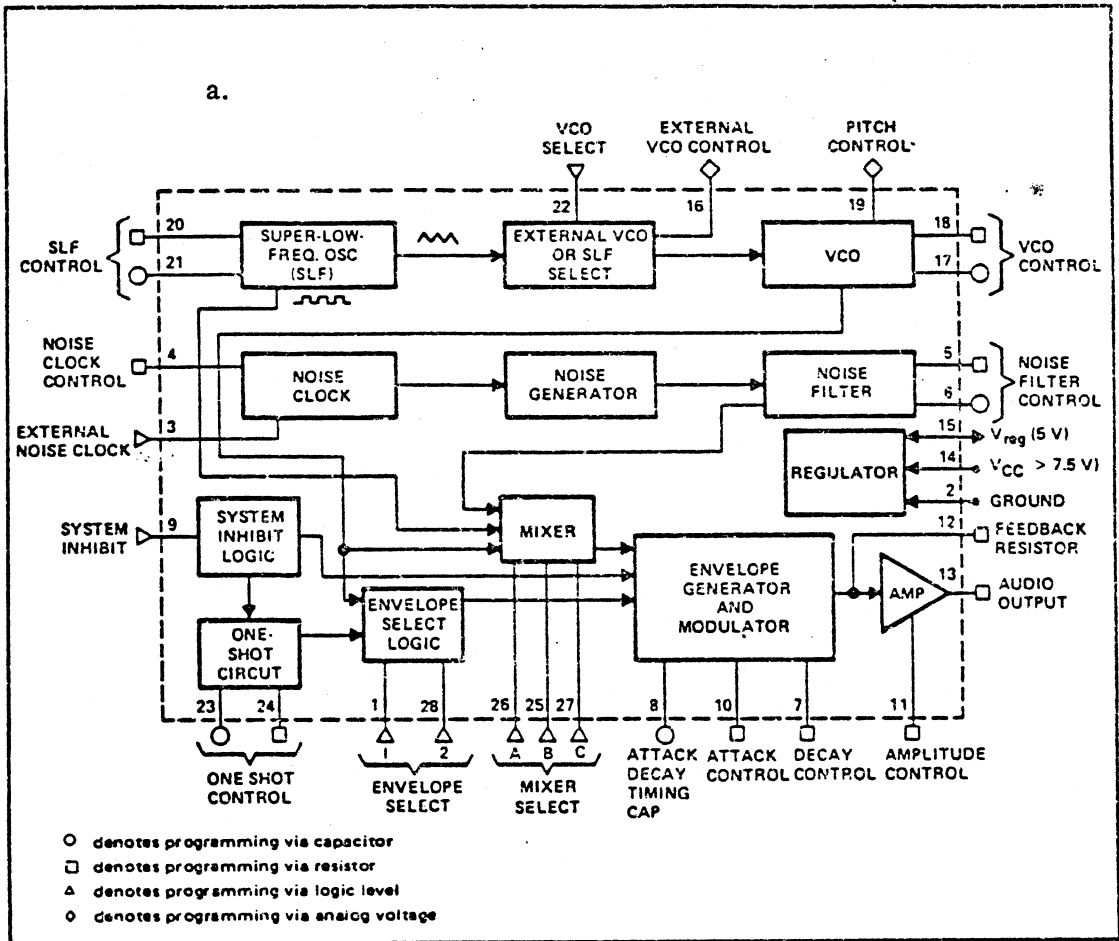
A	B	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level,
X = irrelevant

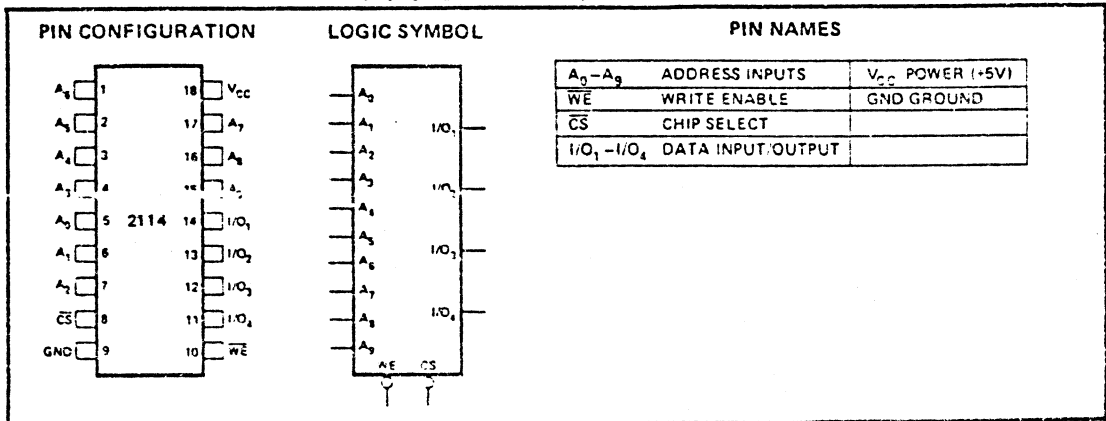


75 189

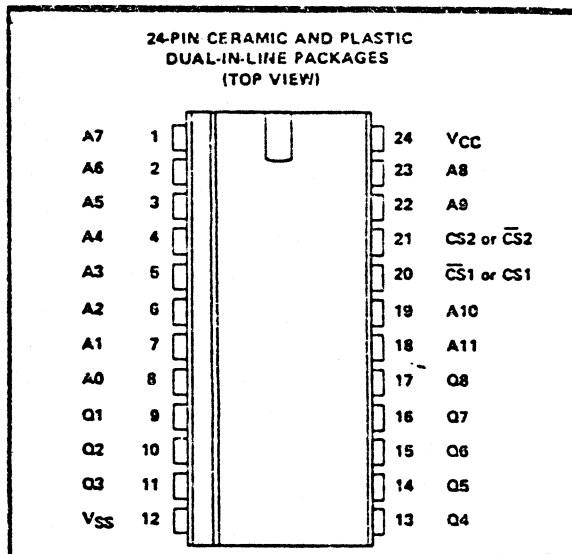




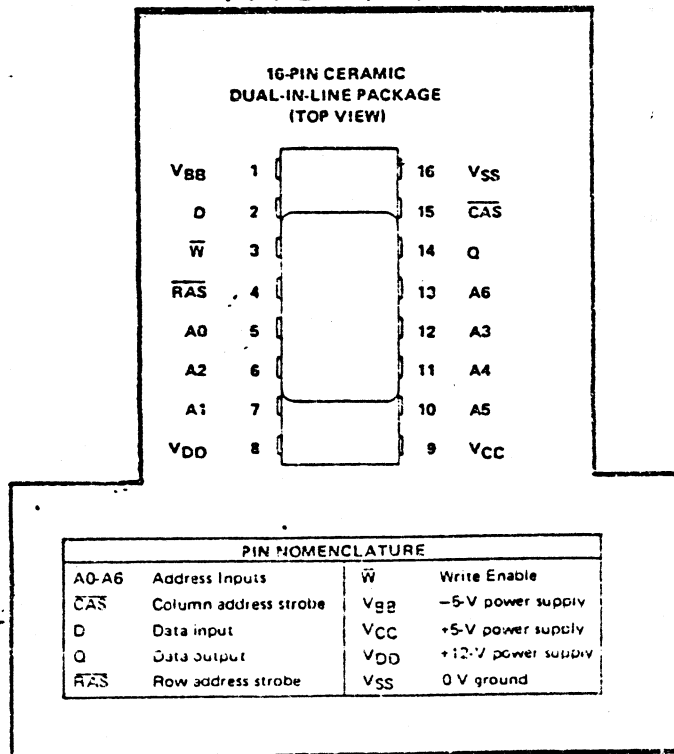
TMS 4045



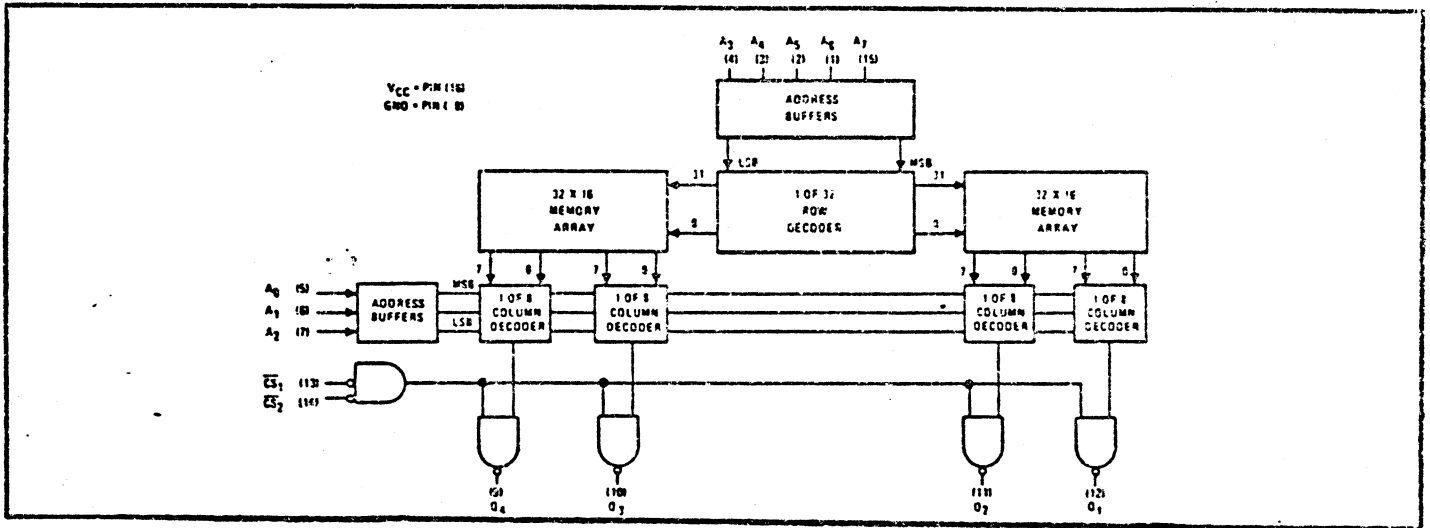
TMS 4732



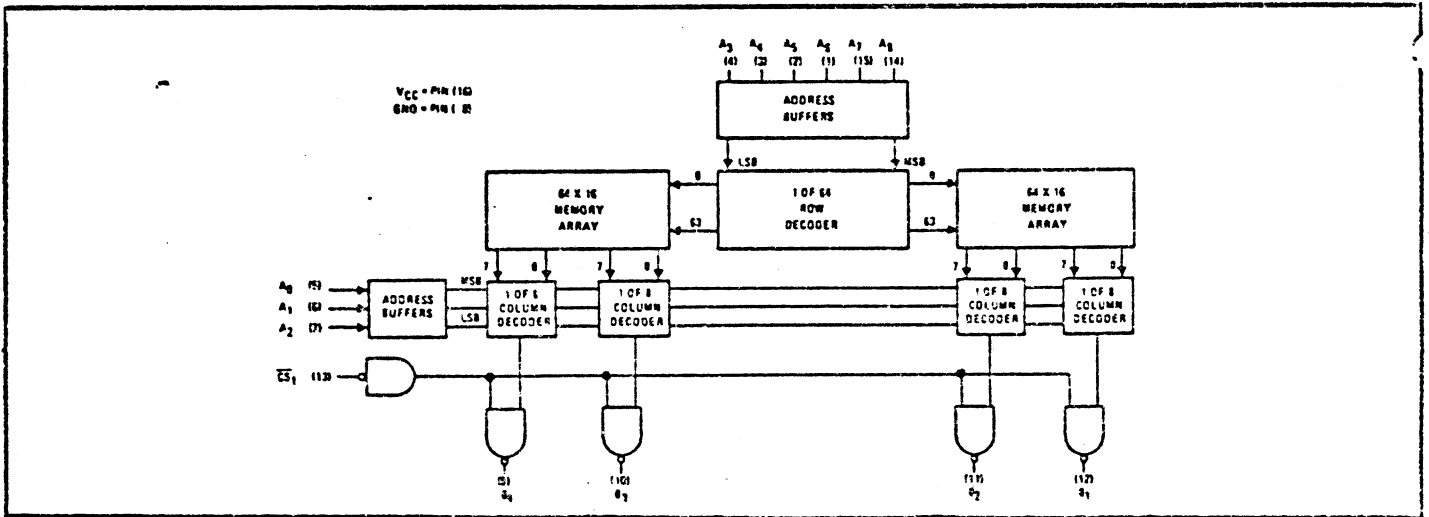
TMS 4116



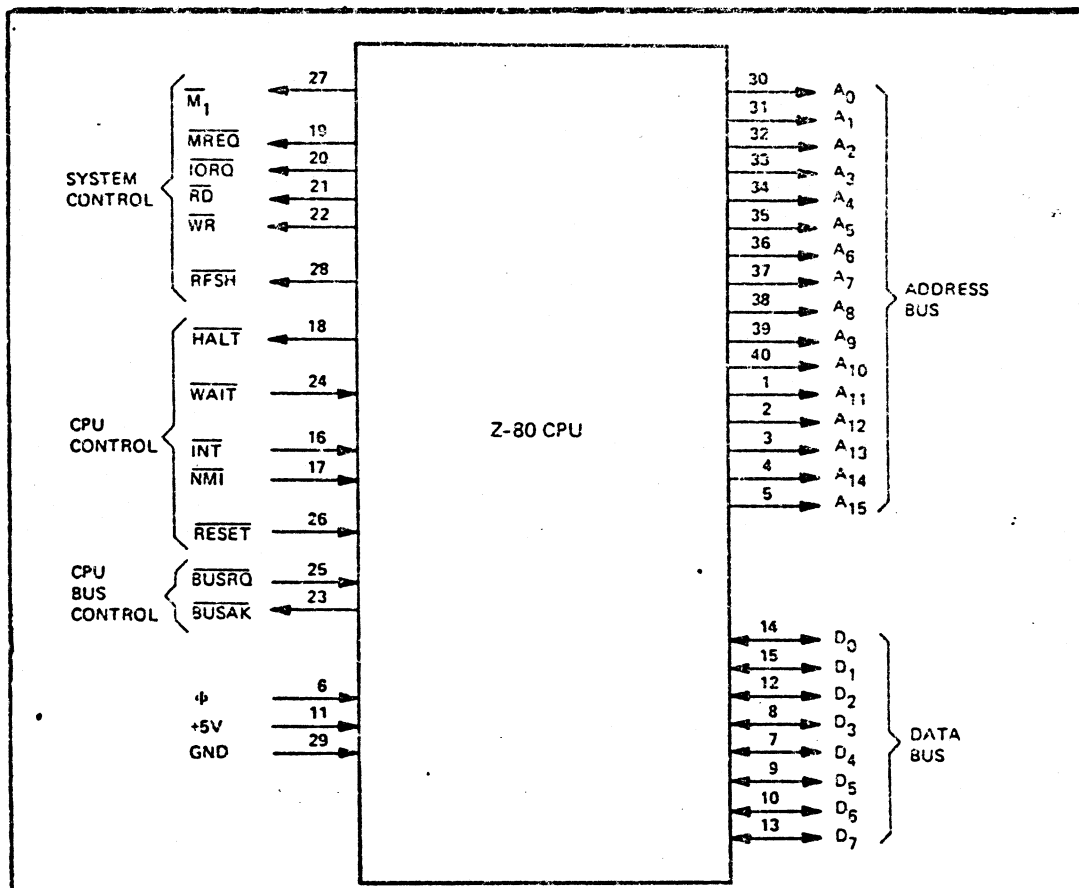
7611



7621



Z 80 CPU

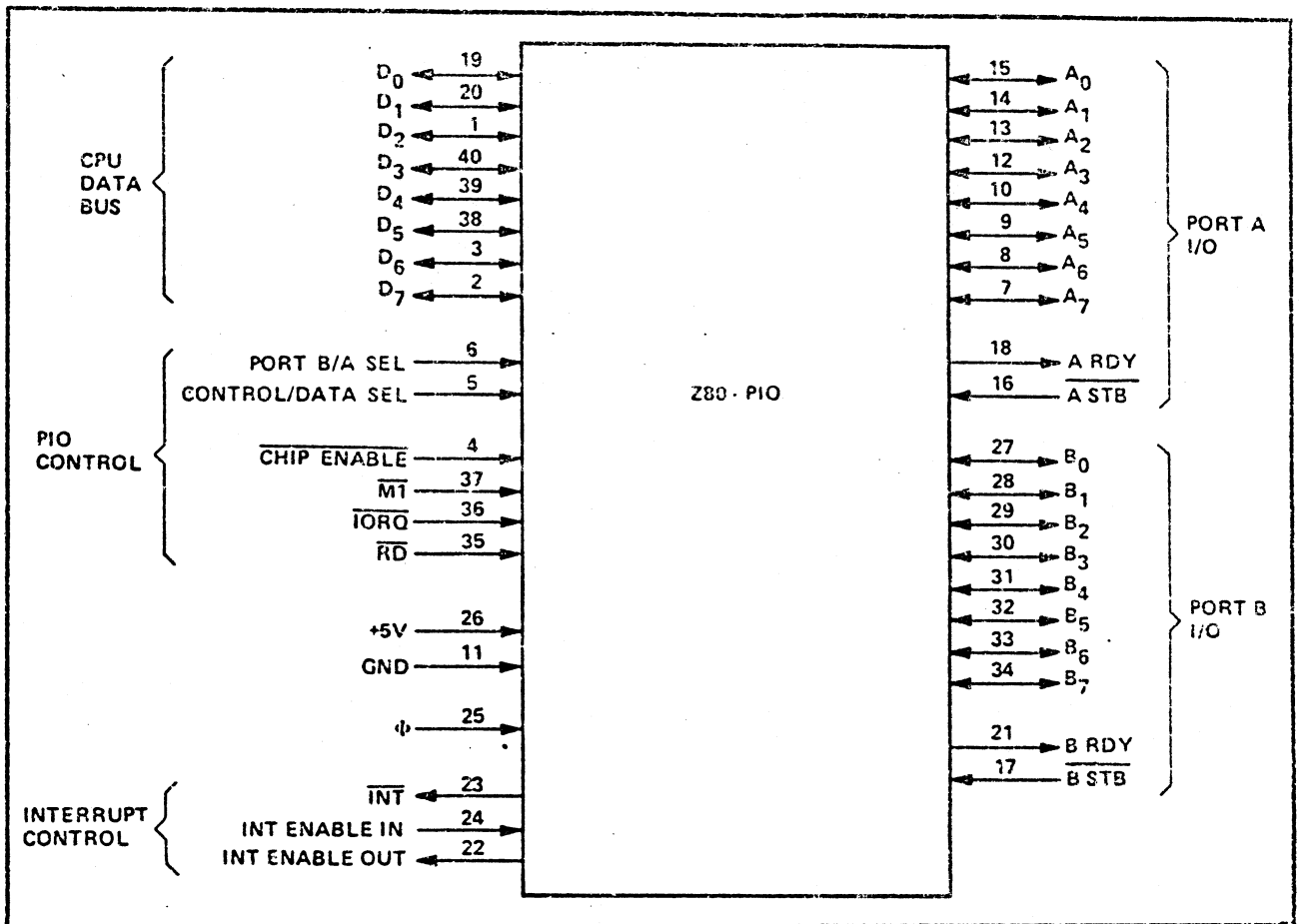


PINBESKRIVNING

- A₀-A₁₅** 16 bitars adressbus tillåter adressering upp till 64 k minne. TRISTATE.
- D₀-D₇** 8 bitars bidirektionell databus för dataöverföring mellan minne, CPU och I/O enheter. TRISTATE.
- M₁** (Machine Cycle One) Indikerar att pågående maskincykel är "fetch OP-code"-cykeln för en instruktion.
- MREQ** (Memory Request) Indikerar att adressbussen innehåller giltig adress för minne eller I/O. TRISTATE.
- IORQ** (Input/Output Request) Indikerar att adressbussens 8 lägsta bitar innehåller giltig I/O adress. Då IORQ uppträder samtidigt med M₁ innebär detta att CPU:n har mottagit avbrottsignal och en avbrottsvektor kan placeras på databussen. TRISTATE.
- RD** (Memory Read) Indikerar att CPU:n skall läsa in data från minne eller I/O. TRISTATE.
- WR** (Memory Write) Indikerar att CPU:n skall skriva data i minne eller I/O. TRISTATE.
- RFSH** (Refresh) Indikerar att de 7 lägsta adressbitarna innehåller refreshadress för dynamiska minnen.

- HALT** (Halt state) Indikerar att CPU:n har utfört en haltinstruktion och väntar på interrupt. (Refresh-aktiviteten uppehålls).
- WAIT** (Wait) Används för att låta CPU:n vänta på långsamma minnen eller I/O.
- INT** (Interrupt Request) Maskerbart avbrott, genereras av I/O-enhet. Avbrott accepteras om avbrottsflaggan ej är aktiv och om NMI ej är aktiv.
- NMI** (Non Maskable Interrupt) Omaskerat avbrott genereras av I/O-enhet. NMI har högre prioritet än INT. Avbrott accepteras alltid oberoende av avbrottsflaggans status.
- RESET** Initierar CPU:n som följer: avbrottsflaggan inaktiveras, programräknaren, I- och R-registren sätts till noll. Interrupt sätts till 8080A-moden.
- BUSRQ** (Bus Request) Tvingar adressbuss, databuss och alla Tri-state-signaler till högimpedivt tillstånd. Används då ett yttre system eller en yttre enhet vill begära tillgång till adress, data och vissa kontroll ledningar.
- BUSAK** (Bus Acknowledge) Indikerar att CPU:n har svarat på en BUSRQ och att alla Tri-state ledningar ligger i det högimpediva tillståndet.
- φ** Systemklocka, ingång, standardfrekvens 4 MHz, enfas TTL-klocka.

Z80 PIO



PINBESKRIVNING

D_0 - D_7 Z80-CPU:ns databuss 8 bitar (bidirektionellt, Tri-state)

B/A SEL Portval, A eller B

C/D SEL Indikerar att databussen innehåller ett Kontrollord/Dataord

M_1 (Machine cycle one) indikerar början av varje instruktion

IORQ (I/O Request) indikerar att adressbussens 8 lägsta bitar innehåller giltig I/O adress. Om IORQ uppträder samtidigt med M_1 , innebär detta att CPU:n har mottagit interruptsignal och en interruptvektor kan placeras på databussen. (Tri-state)

RD (Memory Read) indikerar att CPU:n skall läsa in data från minne eller I/O (Tri-state)

IEI (Interrupt Enable in)

IEO (Interrupt Enable Out) IEI och IEO används för att hårdvarumässigt bilda en interruptprioriteringskedja

INT (Interrupt Request) maskierbar

A STB Port A strobe, puls från periferiutrustning

B STB Port B strobe, puls från periferiutrustning

CE "Chip Enable"

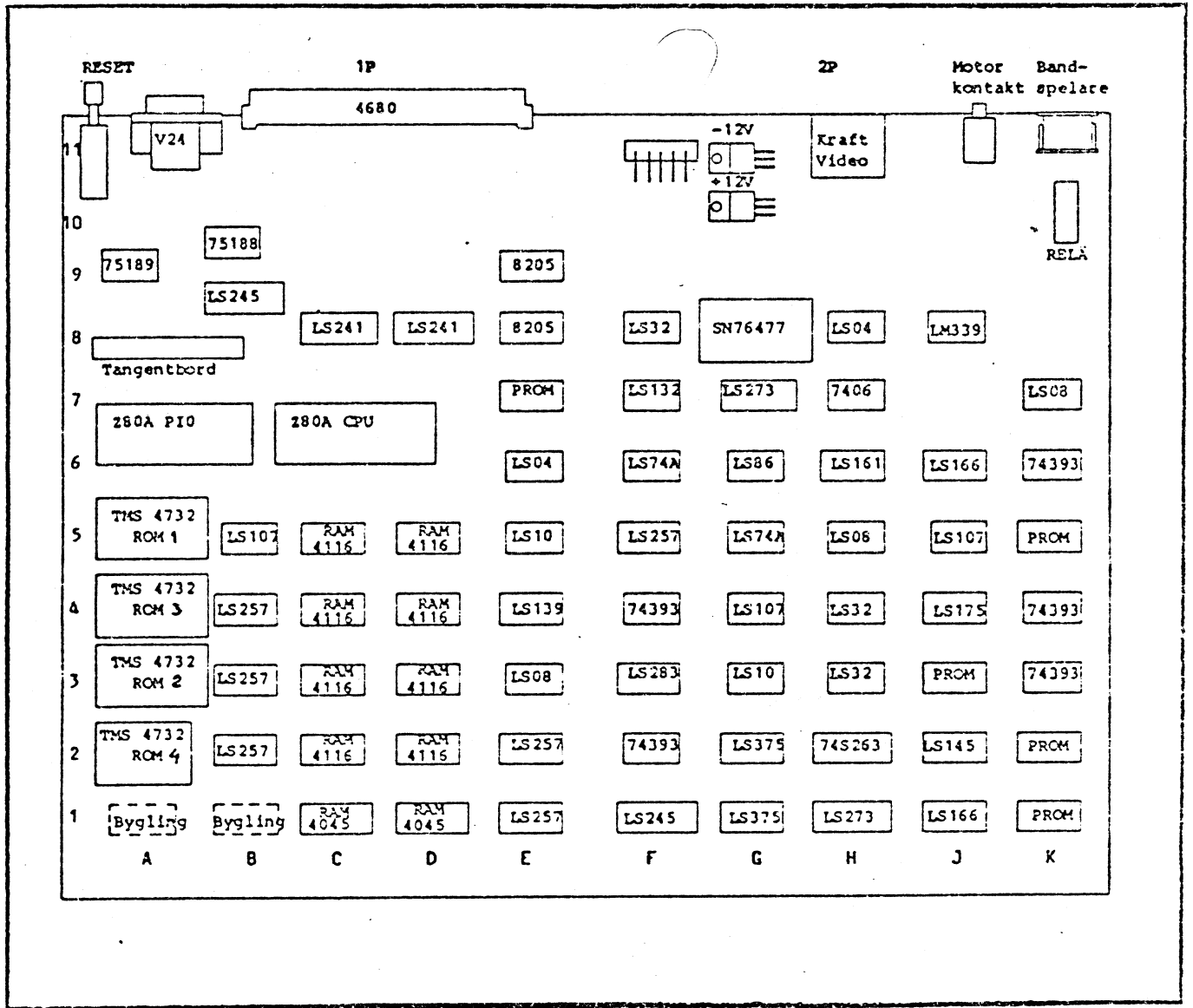
Φ Systemklocka

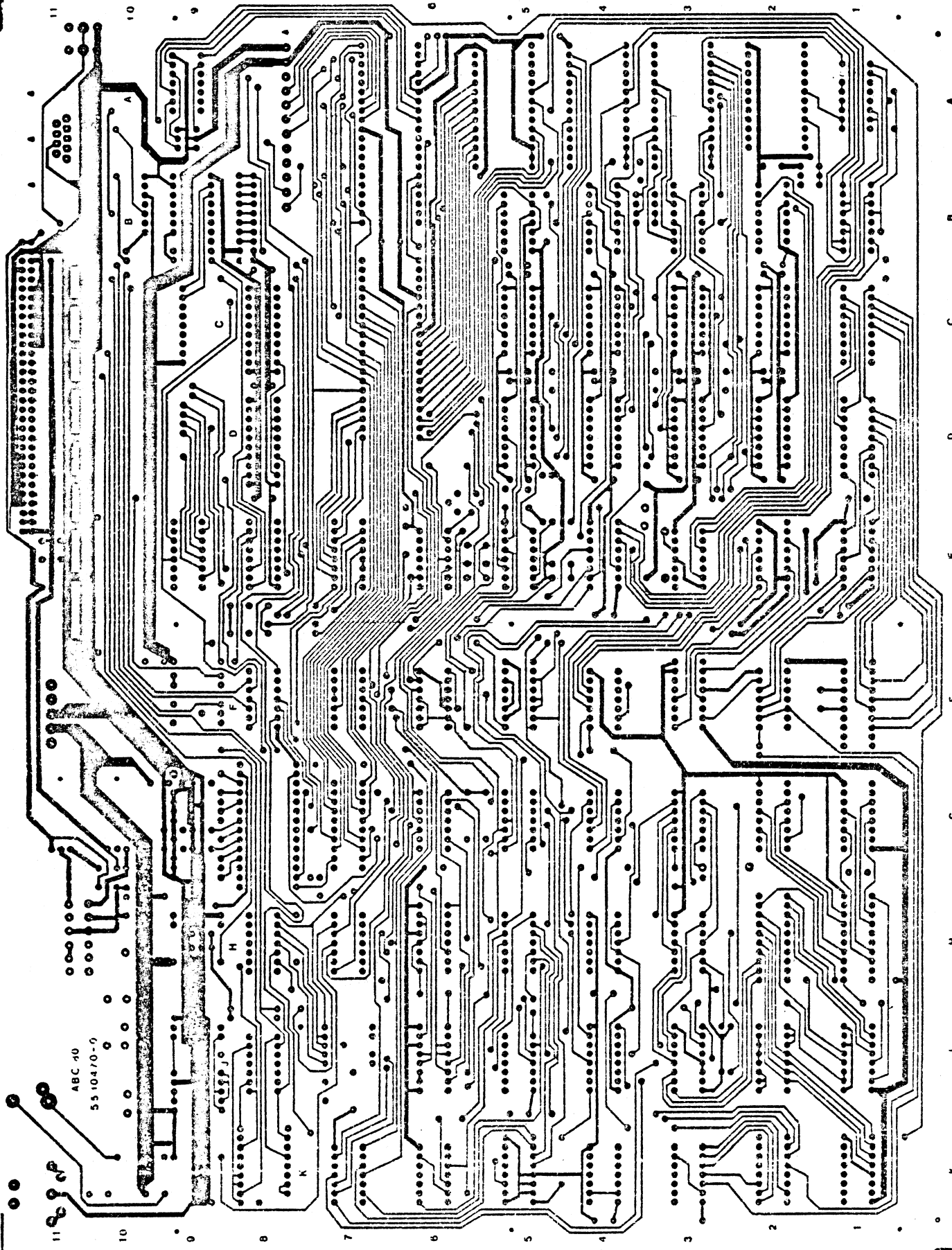
A_0 - A_7 Port A bus

B_0 - B_7 Port B bus

A RDY Register A Ready

B RDY Register B Ready

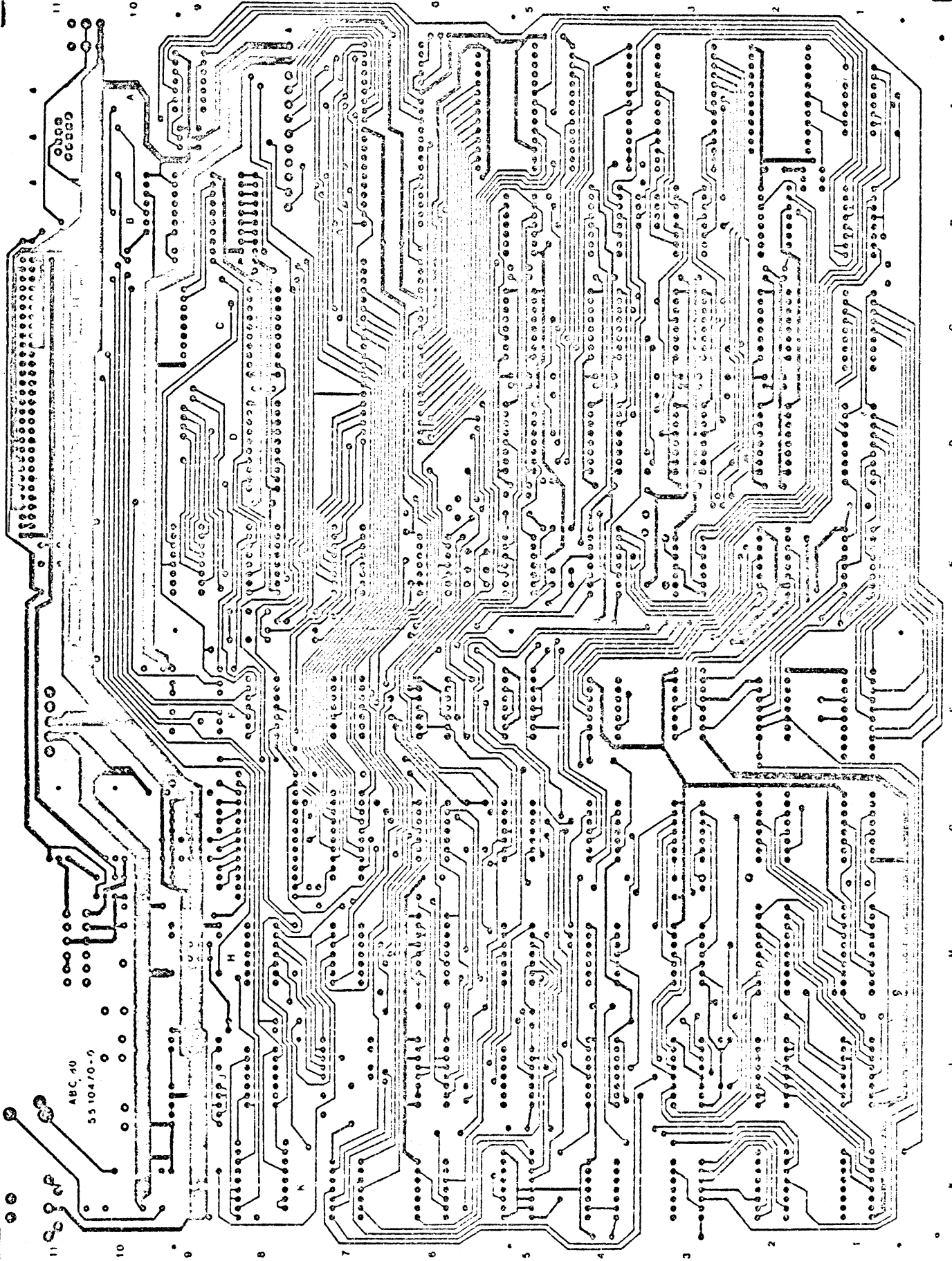




A B C D E F G H J K
 1 2 3 4 5 6 7 8 9 10 11

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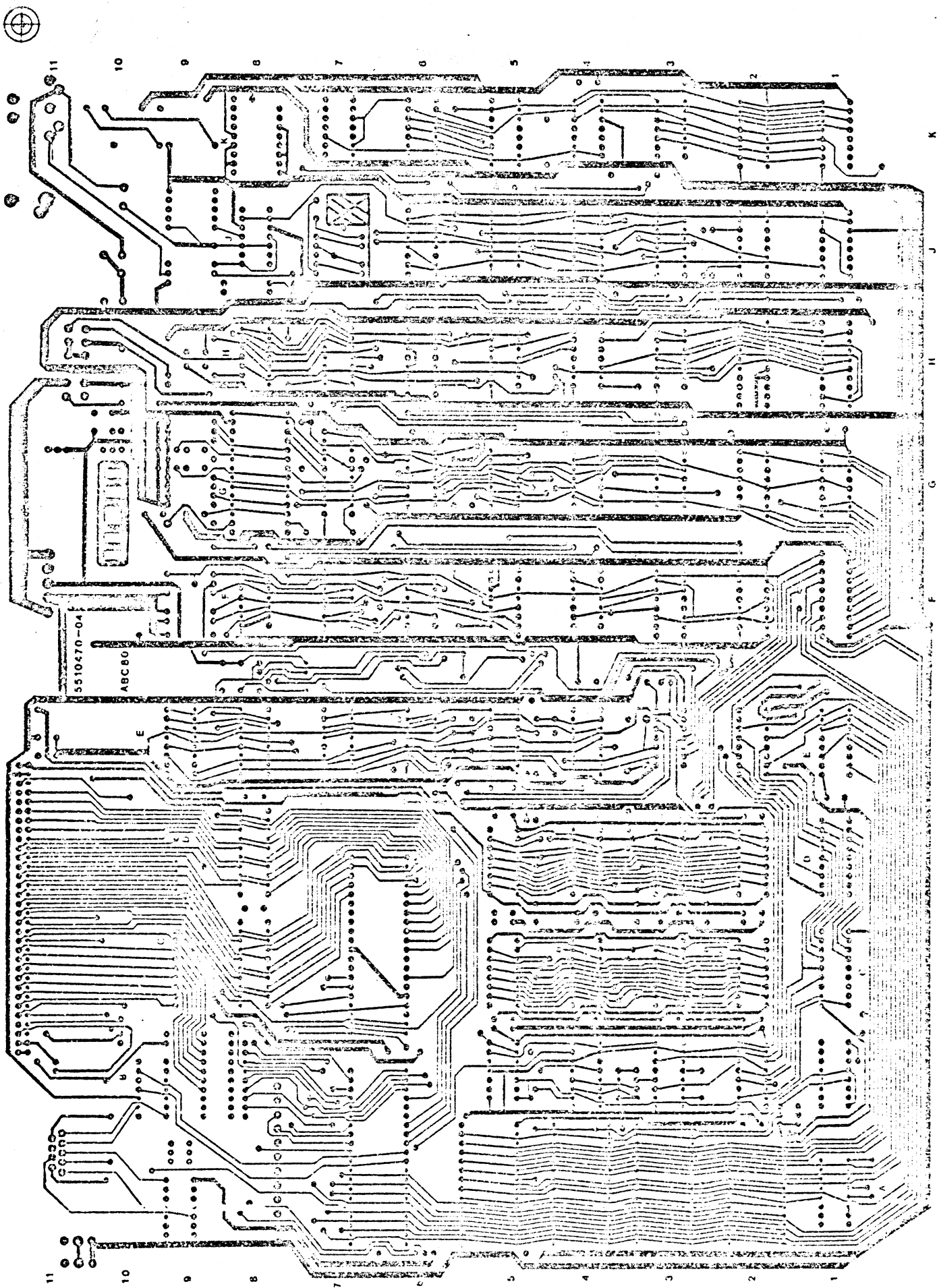
ABC 40 55 10470-0



A B C D E F G H J K

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