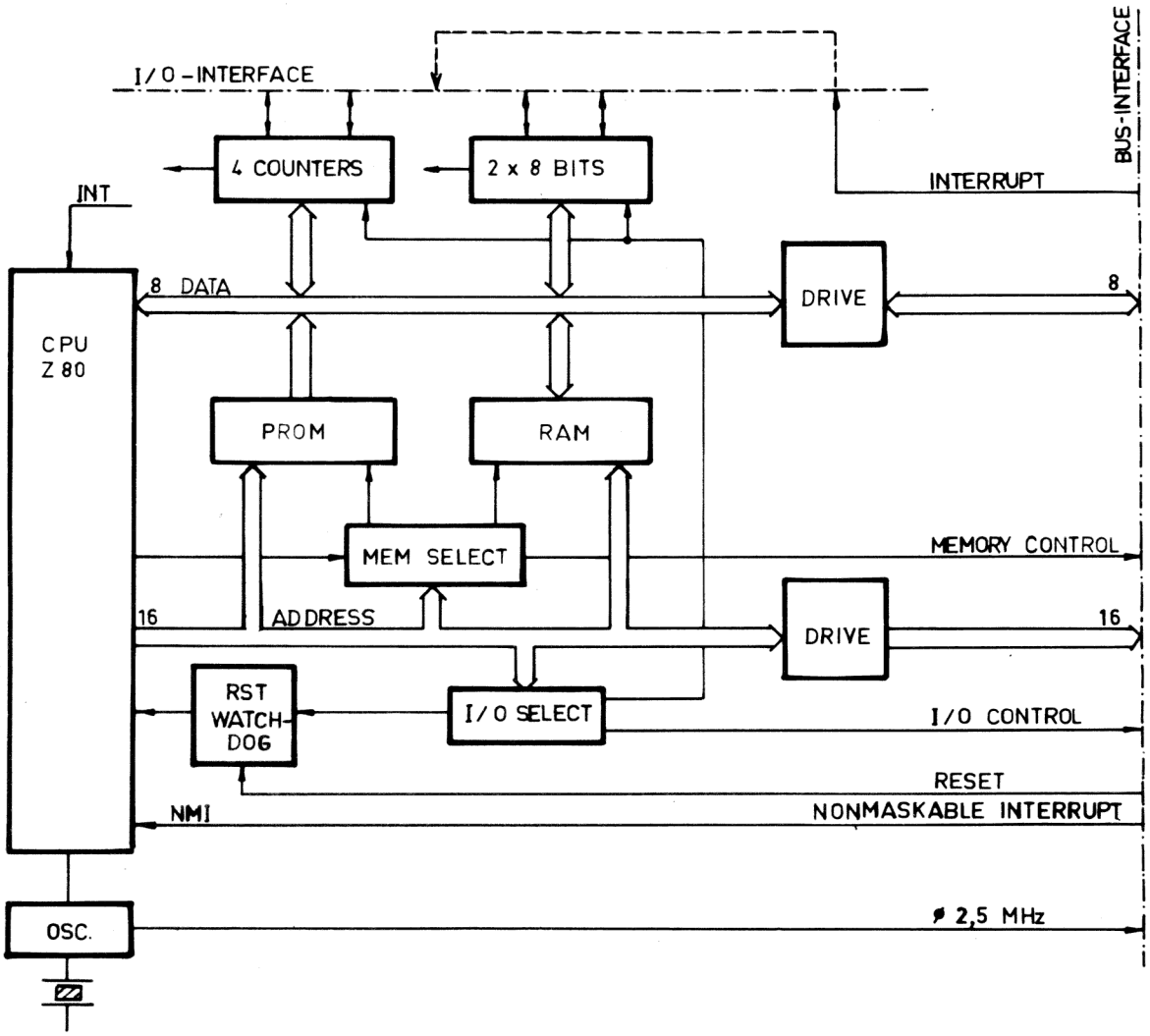

DESCRIPTION

1057 is a single board computer based on Z 80 CPU, CTC and PIO. It comprises interfacing to 4680-bus and direct on-board I/O(counters and universal parallell I/O). 1057 is designed to be used in small applications with the required memory on-board. Memory and I/O-expansion is done through the 4680-bus.

The single board computer does not include use of dynamic RAM and DMA. The double board computer 1043/1044 is chosen in these cases and when more than 2 interrupt levels are required.

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SPECIFICATIONS

NUMBER OF INSTRUCTIONS:		158, includes 4, 8 and 16 bit operations.
CYCLE TIME:		1,6 µs for register to register operations
MEMORY:	**PROM**	2 sockets for any of the types 2708, 2716, 2732 or 2758. The on-board capacities of 2, 4, 8 and 2 kbytes are correspondently provided.
	RAM	1 kbytes static RAM, type 2114.
MEMORY ADDRESSING		
	ON-BOARD PROM	see "options".
	RAM	FC00H - FFFFH
MEMORY EXPANSION		Up to 64 kbytes of RAM:s and (E)(P) ROM:s in any combination through the 4680-bus. Use standard modules from DataBoard 4680.
I/O CAPACITY		2 digital I/O ports of 8 bits and "handshake" signalling on each. Counters (clocks), 4 trigger inputs and 3 outputs.
I/O EXPANSION		Max 64 channels (normally the same in cards).
INTERRUPTS		2 levels NMI, nonmaskable interrupt INT, common level for I/O.
PROGRAM CONTROL		Through watch-dog. Time-out on at least 1 sec. if not operated.
REAL TIME CLOCK		Provided through on-board counter on system or external clock.
SYSTEM CLOCK		2,5 MHz, crystal controlled.
INTERFACING		Both the I/O and bus interfaces are TTL-compatible. All bussignals are buffered. The I/O-signals can be buffered with PIO booster 5057.
POWER		+ 5V ± 5 %, 1,4A (excluding PROM) If 2708 PROM then also "–5V options" including: +12V ± 5 % – 12V ± 5 %
CONNECTOR		64 pin two-row Europe connector (DIN 41612) on both I/O-and bus-sides.
ENVIRONMENT		Operating 0 - + 55 ^{o} C

INTERRUPT

The interrupt handling is connected to and completely controlled by the internal I/O. Interrupt signalling from the I/O-bus is available through the NMI - or INT-signals. The INT -signal is drawn to the I/O-connector from which it can be returned by a jumper via any of the internal ports. The input of counter O provides the highest priority (next to NMI) and dataport B (mode 3) the lowest.

The nonmaskable interrupt (NMI) initiates a subroutine call by 66H. "Power-down" may for example be connected to the NMI for fastest response.

The INT-interrupt is mode-controlled. The programmer determines the mode and loads CTC and PIO with appropriate vectors. Further information is provided in System Manual.

RESTART

This function is available through internal "program monitoring by hardware" (watch-dog). Restart resets CPU and initiates program run on address O. The function is also activated by "power-on". Manual restart and disconnection of the watch-dog is available via the bus. The input and output functions are reset at "power-on" and provided by a specific out-command.

MEMORY CONTROL

The single board computer provides memory expansion through the 4680-bus interface which contains memory control as follows:

* MEMFL — for memory read
* W — for memory write

and 16 bits address.

When selecting memory the user must consider the maximum total access times given below. The total access time is calculated to the access time of the memory circuit on the module plus standard 100 nsec. for delays (3TTL, bus and CPU).

The maximum total access times allowed are:

1) 550 nsec. - for instruction fetch
2) 750 nsec. - for access of data
3) 750 nsec. - for input/output operations

4680- BUS INTERFACING

Standard and flexible expansion is provided through ready to use backplanes. 8, 14 and 20 slot racks are available. The user has also the choice of wiring the backplane himself. Bus-wiring and -signals are presented in the System Manual.

The single board computer may use the backplanes of the double board computers by plugging 1057 into the Control Unit slot and a jumper board into the CPU slot. See System Manual.

The 8-slot backplane is designed for single board computers only.

PIN NUMBERING - INTERNAL I/O

2 x 8 bits

Signal	A-data (7-0)	strobe	ready	B-data (7-0)	strobe	ready
Pin	18B - 25B	26B	28B	21A - 28A	27B	29B

4 counters

Signal	O IN	O OUT	1 IN	1 OUT	2 IN	2 OUT	3 IN
Pin	5B	6B	6A	7B	7A	8B	8A

Interrupt pin 29A **Signal earth** pin 2A, 2B

OPTIONS

Selection of PROM - type and memory segment for on-board memory:

2708	b 1 c,	b 2 c,	b 3 (inserted)	and	b 4 (inserted)	0 - 7FFH
2716	b 1 b,	b 2 b,	b 3 (open)	and	b 4 (inserted)	0 - FFFH
2732	b 1 b,	b 2 a,	b 3 (inserted)	and	b 4 (open)	0 - IFFFH
2758	b 1 a,	b 2 b,	b 3 (inserted)	and	b 4 (inserted)	0 - 7FFH
no on-board memory			b 3 (open)	and	b 4 (open)	-

Ref.

The System Manual present the DataBoard con cept and provides details on system functions, bussignalling etc.

I/O CONTROL

Is standard DataBoard 4680 I/O-bus signalling. See System Manual. It comprises control of watch-dog and I/O-reset. Internal on-board I/O, the counters and the 8 - bit ports, are not included in normal 4680 I/O-commanding. These are operated in correspondance with the product specifications of Z 80 - CTC and -PIO. Running operations on the I/O - bus can be multiplexed with the on-board I/O without disturbances form each other. The channel selection on I/O- bus stands unchanged.

The addresses of internal I/O are as follows:

Counter	0	1	2	3
Address	30H	31H	32H	33H

Port	A-data	A-control	B-data	B-control
Address	38H	39H	3AH	3BH

ON-BOARD LOCATION OF JUMPERS AND OPTIONS