KEYEX

TEAC FD-55F
MINI FLEXIBLE DISK DRIVE
SPECIFICATION

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ÄNDRING TILL 40 SPÅR

R 14 = 10 Ω

1-1. APPLICATION

This SPECIFICATION provides a description for the TEAC FD-55F, double sided 96tpi mini flexible disk drive (hereinafter referred to as the FDD).

1-2. DISK

5.25 inch, soft or hard sectored flexible disks which are mutually agreed between the customer and TEAC.

1-3. PHYSICAL SPECIFICATION

(1) Width: 146mm (5.75 in), Nom.

(2) Height: 41.3mm (1.63 in), Nom.

(3) Depth: 203mm (7.99 in), Nom. (excludes projections of interface connectors)

(4) Weight: 1.5Kg (3.31 lbs) or less

(5) External view: See Fig.101

(6) Cooling: Natural air cooling

(7) Mounting: Mounting for the following directions are acceptable.

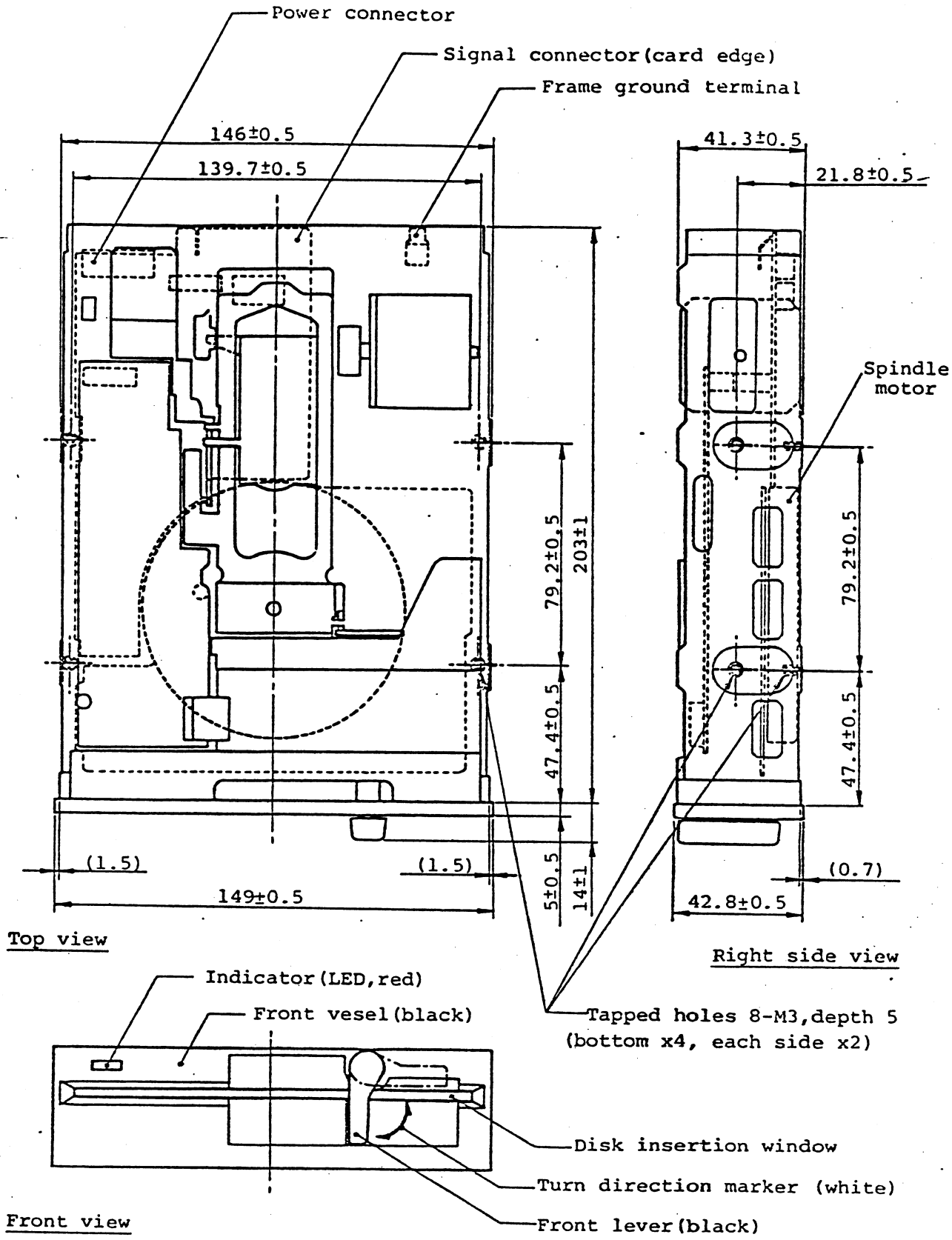
(a) Front loading, mounted vertically with front lever up or down.
(b) Front loading, mounted horizontally with indicator up. Do not mount horizontally with spindle motor up.
(c) Mounting angle in items (a) and (b) should be less than 15° with front vessel up.

Note: As to the most appropriate mounting condition and mounting for other directions than the above will be considered separately.

(8) Installation: With installation holes on the side frame or on the bottom frame of the FDD (see Fig.101)

(9) Material of frame: Aluminum diecast

(10) Material of front vessel: ABS
Standard color : Munsell N1, black



(Units:mm)

(Fig.101) External view

1-4. REQUIRED POWER

The following specifications are applicable at the power connector of the FDD.

(1) DC+12V

(a) Voltage tolerance

Read/write operation: Less than ±5%

Others : Less than ±10%

(b) Allowable ripple voltage: Less than 200mVp-p (including noise)

(c) Operating current consumption

Typical average: 0.25A

(using a disk of typical running torque)

Maximum average: Less than 0.6A

(using a disk of maximum running torque)

Peak: Less than 0.9A (400msec, Max. at spindle motor start)

(d) Waiting current consumption (spindle motor off)

Typical: 0.05A

Maximum: 0.08A

(2) DC+5V

(a) Voltage tolerance: ±5%

(b) Allowable ripple voltage: Less than 100mVp-p (including noise)

(c) Operating current consumption

Typical average: 0.5A

Maximum average: Less than 0.65A

Peak: Less than 0.8A

(d) Waiting current consumption

Typical: 0.4A

Maximum: Less than 0.5A

(3) Power consumption

(a) Typical at operating: 5.5W

(b) Typical at waiting: 2.6W

(4) Power on sequence

Not specified. Since the FDD is equipped with power reset circuit, disk and data on the disk will not be damaged by power on or off.

1-5. ENVIRONMENTAL CONDITIONS

(1) Ambient temperature

(a) Operating: 4°C ∿ 46°C (40°F ∿ 115°F)
(b) Storage: -22°C ∿ 60°C (-8°F ∿ 140°F)
(c) Transportation: -40°C ∿ 65°C (-40°F ∿ 149°F)

(2) Temperature gradient

(a) Operating: Less than 15°C (27°F) per hour
(b) Transportation and storage: Less than 30°C (54°F) per hour

(3) Relative humidity

(a) Operating: 20% ∿ 80% (no condensation)
Maximum wet bulb temperature: 29°C (84°F)
(b) Storage: 10% ∿ 90% (no condensation)
(c) Transportation: 5% ∿ 95% (no condensation)

(4) Vibration

(a) Operating: Less than 0.25G (5 ∿ 150Hz)
(b) Transportation: Less than 2G (5 ∿ 100Hz)

(5) Shock

(a) Operating: Less than 10G (Less than 10msec)
(b) Transportation: Less than 40G (Less than 10msec)

(6) Altitude

(a) Operating: Less than 5,000m (16,500 feet)
(b) Transportation: Less than 12,000m (40,000 feet)

1-6. OPERATIONAL CHARACTERISTICS

(1) Data capacity

Recording method			FM	MFM
Data transfer rate (K bits/sec)			125	250
Tracks/disk			160	160
Innermost track bit density (bpi)			2,961(side 1)	5,922 (side 1)
Innermost track flux density (frpi)			5,922(side 1)	5,922 (side 1)
Data capacity	Unformatted	K bytes/track	3.125	6.25
		K bytes/disk	500	1,000
	Formatted (16 sectors /track)	K bytes/sector	0.128	0.256
		K bytes/track	2.048	4.096
		K bytes/disk	327.68	655.36

(Table 101) Data capacity

(2) Disk rotation mechansim

(a) Spindle motor: Direct DC brushless motor

(b) Spindle motor speed: 300rpm

(c) Motor servo method: Frequency servo by AC tachometer

(d) Motor/spindle connection: Motor shaft direct

(e) Disk speed: 300rpm

Long term speed variation (LSV): Less than ±1.5%

Instantaneous speed variation (ISV): Less than ±1.5%

(f) Start time: Less than 400msec

(g) Average latency: 100msec

(3) Index

(a) Number of index: 1 per disk revolution

(b) Detection method: LED and photo-transistor

(c) Detection cycle: 200msec ± 1.5%

(d) Index/alignment dipole spacing: 0 ∿ 400μsec, with specified test disk.

(4) Track construction

(a) Track density: 96tpi
(b) Number of cylinders: 80 cylinders
(c) Number of tracks: 80 tracks/surface, 160 track/disk
(d) Outermost track radius (track 00): Side 0 57.150mm (2.2500 in)
Side 1 55.033mm (2.1667 in)
(e) Innermost track radius (track 79): Side 0 36.248mm (1.4271 in)
Side 1 34.131mm (1.3438 in)
(f) Positioning accuracy: Less than ±20μm, with specified test disk.
(Track 32, 23±2°C, 40 ∿ 60%RH)

(5) Magnetic head

(a) Magnetic head: Gimball supported read/write head with tunnel erase, 2 sets
(b) Read/write head track width: 0.160mm (0.0063 in), Nom.
(c) Effective track width after tunnel erase:
0.150 ± 0.015mm (0.0059 ± 0.0006 in)
(d) Erase head track width: 0.100mm (0.0039 in), Nom.
(e) Read/write-erase gap spacing: 0.85 ± 0.05mm (0.0335 ± 0.0020 in)
(f) Read/write gap azimuth: 0° ± 18', with specified test disk.

(6) Track seek mechanism

(a) Head positioning mechanism: Band positioner
(b) Stepping motor: 4-phase, 200 steps per revolution
(c) Stepping motor drive: 1 step per track
(d) Outermost and innermost stopper: Mechanical moving stopper of head carriage
(e) Track 00 detection method: LED and photo-transistor
(f) Track to track time: Less than 3msec
(g) Settling time: Less than 15msec (excludes track to track time)
(h) Average track access time: 94msec (includes settling time)

(7) Head load mechanism

(a) Head load mechanism: Plunger solenoid

(b) Head load time: Less than 35msec

(8) File protect mechanism: Detection of write enable notch by LED and photo transistor

(9) Window margin (shipping): More than 600nsec, with specified test disk, MFM method, PLO separator, and 0 write pre-compensation.

1-7. RELIABILITY

(1) MTBF: 10,000 power on hours or more (for typical usage)

(2) MTTR: 30 minutes

(3) Design component life: 5 years

(4) Preventive maintenance: Not required (for typical usage)

(5) Error rates

(a) Soft read error: 1 per 10^9 bits (up to 2 retries)
(b) Hard read error: 1 per 10^{12} bits
(c) Seek error: 1 per 10^6 seeks

(6) Security standard: Complying with UL, CSA

1-8. SIGNAL INTERFACE

Four FDDs, Max. can be connected to one FDD controller by daisy chaining.

1-8-1. Electrical Characteristics

(1) Interface driver/receiver: See Fig.102.

(2) Electrical characteristics

The following specifications are applicable at the signal connector of the FDD.

(a) Input signal

LOW level (TRUE): 0V ∿ 0.5V

Terminator current: 18mA, Max.

Receiver TTL current: 3.2mA, Max.

HIGH level (FALSE): 2.5V ∿ 5.25V

(b) Output signal

LOW level (TRUE): 0V ∿ 0.4V

Driver sink current capability: 48mA, Max.

HIGH level (FALSE): 5.25V, Max.

(depending on controller terminator)

(3) Terminator

(a) Resistance value: 330Ω ± 5%

(b) Terminator for DRIVE SELECT 0 ∿ 3 input signals:

A terminator resistor is mounted on the PCB with soldering joint.

(c) Terminator for other input signals:

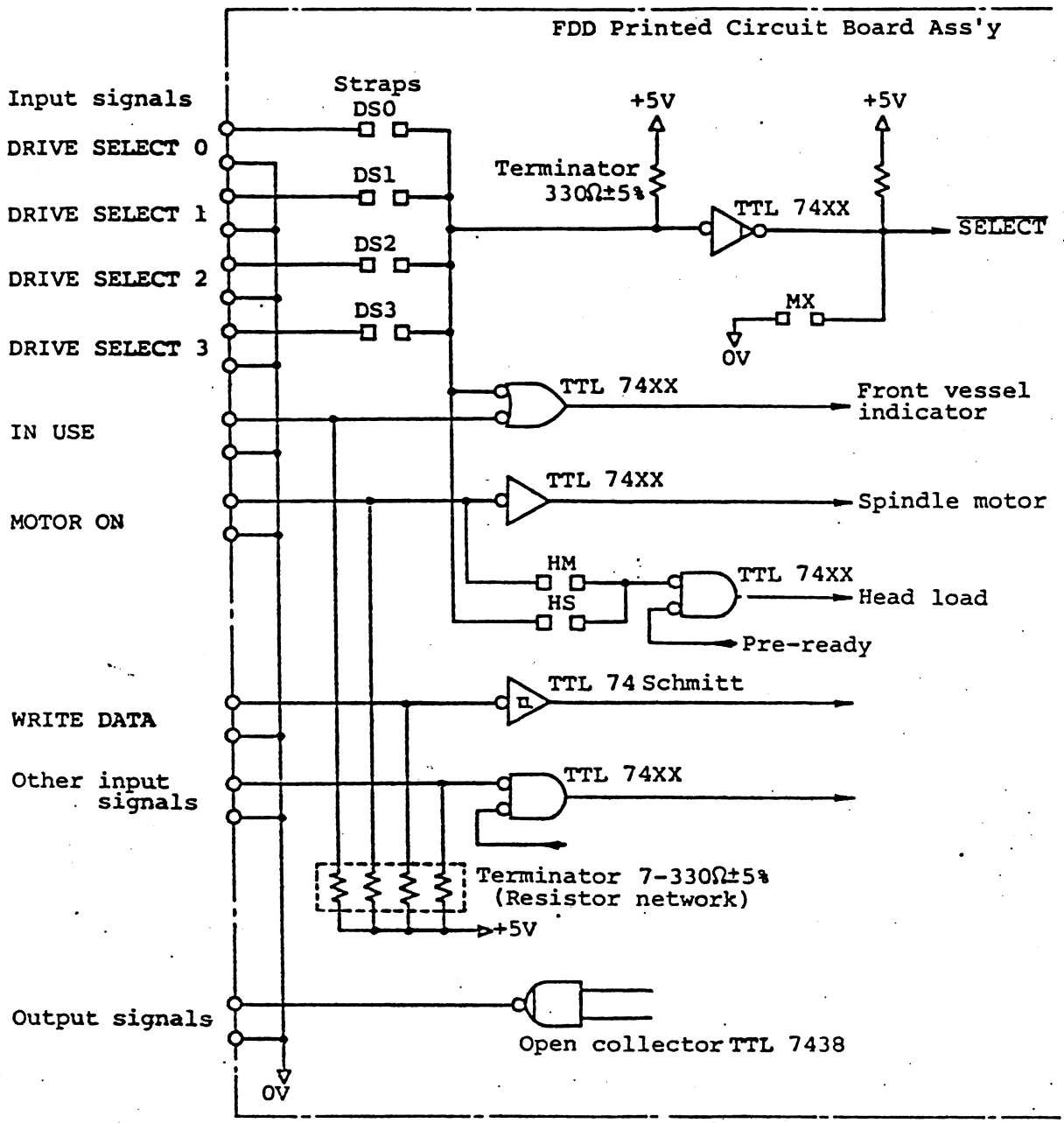
A resistor network is mounted on IC socket on the PCB.

(d) Shipping condition

All of the terminator resistors are mounted.

(e) Multiplex connection:

For the multiplex connection of the FDDs by daisy chaining, the resistor network explained in item (c) shall be removed from all the FDDs except for the final FDD of the interface cable.



(Fig.102) Signal interface circuit

1-8-2. Signal Connector and Cable

(1) Signal connector

(a) FDD side connector: Card edge (gold plated)

(b) Pin numbers & pin pitch: 34 pins, 2.54mm (0.1 in) pitch
(17 pins on both sides, even number pins are bottom side of the FDD)

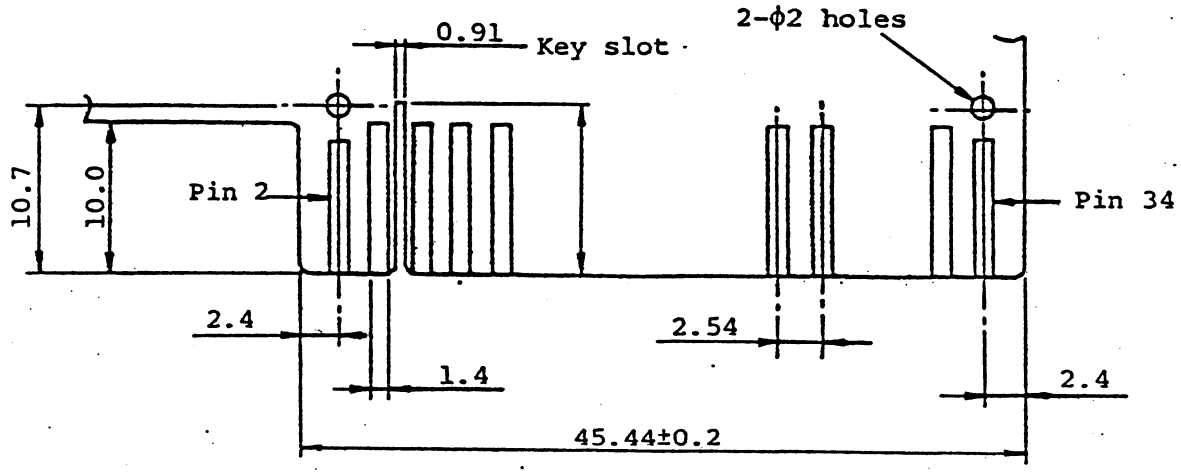
(c) Polarizing key location: Between pins 4 and 6

(d) Card edge dimensions: See Fig.103

(e) Interface connections: See Table 102

(f) Cable side matched connector: 3M, Scotchflex ribbon connector, P/N 3463-0001
or AMP, thin leaf connector, P/N 583717-5 and contactor P/N 1-583616-1
or equivalent

(2) Maximum interface cable length: 3m, Max.
For the multiplex connection by daisy chaining, the total cable length shall be less than 3m.



Notes: 1. PCB thickness: 1.6mm, Nom.
2. The figure shows bottom view of the FDD.

(Fig.103) Card edge dimensions of signal connector

Signals	Directions	Terminal Nos.	
		Signals	0V
SPARE	INPUT	2	1
IN USE	INPUT	4	3
DRIVE SELECT 3	INPUT	6	5
INDEX/SECTOR	OUTPUT	8	7
DRIVE SELECT 0	INPUT	10	9
DRIVE SELECT 1	INPUT	12	11
DRIVE SELECT 2	INPUT	14	13
MOTOR ON	INPUT	16	15
DIRECTION SELECT	INPUT	18	17
STEP	INPUT	20	19
WRITE DATA	INPUT	22	21
WRITE GATE	INPUT	24	23
TRACK 00	OUTPUT	26	25
WRITE PROTECT	OUTPUT	28	27
READ DATA	OUTPUT	30	29
SIDE ONE SELECT	INPUT	32	31
READY	OUTPUT	34	33

Note: SPARE terminal is open condition.

(Table 102) Signal interface connections

1-8-3. Input/Output Signals

In the following, input signals are those transmitted to the FDD while output signals are those transmitted from the FDD. LOW level of the signals is TRUE.

(1) DRIVE SELECT 0 ∿ 3 input signals

(a) Level signals of four lines to select a specific FDD for operating in multiplex control by daisy chaining.

(b) When the MX strap is off, only the DRIVE SELECT signal of the same number as of on-state strap among DS0 ∿ 3 straps is effective.

(c) All the output signals and all the input signals except for the MOTOR ON and the IN USE signals can be effective when this signal is effectively received or when the MX strap is on.

(d) The time required to make each input or output signal effective after the transmission of this signal is 0.5μsec, Max. including delay time through the interface cable.

(e) When the DRIVE SELECT signal of the same number as of on-state strap among DS0 ∿ 3 straps becomes TRUE (independent of the MX strap), the indicator on the front vessel turns on.
If the HS strap is on at this time and the FDD is in ready or pre-ready state, head loading will be started.
Head loading will be completed within 35msec after this signal becomes TRUE, and then data read or write operation can be executed if the FDD is in ready state. (Refer to item (12)).

(2) MOTOR ON input signal

(a) Level signal to rotate the spindle motor.

(b) The spindle motor reaches to the rated rotational speed within 400msec after this signal becomes TRUE.

(c) When the HM strap is on, head loading will be started after the FDD becomes pre-ready state. Then the FDD becomes ready state, data read

or write operation can be executed immediately. (Refer to item (12)).

(3) DIRECTION SELECT input signal

(a) Level signal to define the moving direction of the head when the STEP line is pulsed.

(b) Step-out (moving away from the center of the disk) is defined as HIGH level of this signal. Conversely, step-in (moving toward the center of the disk) is defined as LOW level of this signal.

(4) STEP input signal

(a) Pulse signal to move the head. The pulse width shall be more than 0.8μsec and the head moves one track space per one pulse.

(b) The access motion (head seek operation) is initiated at the trailing edge of the pulse and completes within 18msec after starting the access including the settling time. For the successive access motion in the same direction, the pulses shall be input with the space of more than 3msec, while the pulses shall be input with the space of more than 18msec for the access motion in a different direction.

(c) This signal becomes ineffective when the WRITE PROTECT signal is FALSE and the WRITE GATE signal is TRUE.

(d) This signal shall be input according to the timing in Fig.104.

(5) WRITE GATE input signal

(a) Level signal to erase the written data and to enable the writing of new data.

(b) This signal becomes ineffective when the WRITE PROTECT signal is TRUE.

(c) This signal shall be made TRUE after satisfying all of the following four conditions.

i) The FDD is in ready state (refer to item (12)).

ii) More than 35msec after the head loading is started.

iii) More than 18msec after the effective receival of the final STEP pulse.

iv) More than 100μsec after the level change of the SIDE ONE SELECT signal.

(d) None of the following operations shall be done for at least 1msec after this signal is changed to FALSE.

i) Make the MOTOR ON signal FALSE.

ii) Make the DRIVE SELECT signal FALSE.

iii) Start the head access motion by the STEP pulse.

iv) Change the level of the SIDE ONE SELECT signal.

(6) WRITE DATA input signal

(a) Pulse signal to designate the contents of the data to be written on the disk. The pulse width shall be more than 0.25μsec and the leading edge of the pulse is used.

(b) This signal becomes ineffective when one of the following conditions is satisfied.

i) WRITE GATE signal is FALSE.

ii) WRITE PROTECT signal is TRUE.

(c) This signal shall be input according to the timing in Fig.105.

(7) SIDE ONE SELECT input signal

(a) Level signal to define which side of a two-sided disk is used for reading or writing.

(b) When this signal is HIGH level, the magnetic head on the side 0 surface of the disk is selected, while the magnetic head on the side 1 surface is selected when this signal is LOW level.

(c) The READ DATA signal on a selected surface becomes valid more than 100μsec after the change of this signal level.

(d) Write operation (WRITE GATE signal TRUE) on a selected surface shall be started more than 100μsec after the change of this signal level.

(e) When the other side of the disk is selected after the completion of

a write operation, the level of this signal shall be switched more than 1msec after making the WRITE GATE signal FALSE.

(8) TRACK 00 output signal

(a) Level signal which indicates that the head is on track 00 (the outermost track).
(b) This signal becomes valid more than 2.8msec after the effective receival of the STEP pulse.
(c) If a step-out command is input at track 00, the head is shifted a little outside from the track 00 position and the TRACK 00 signal becomes FALSE immediately after the input of the STEP pulse. If a step-out command or additional three step-in commands are input at the position, the head correctly returns to the track 00 position and the TRACK 00 signal becomes TRUE.

(9) INDEX/SECTOR output signal

(a) Pulse signal for the detection of the index hole or the sector holes.
(b) This signal becomes valid 400msec after the spindle motor starts rotation.
(c) When using a soft sectored disk, there will be one index pulse on this line per one revolution of the disk. When using a hard sectored disk, sector pulse and index pulse are output together.
(d) Fig.106 shows the timing for this signal. Leading edge of the pulse shall be used as the reference.
(e) If the output condition in item (1)-(c) is satisfied when no disk is inserted, this signal maintains TRUE.

(10) READ DATA output signal

(a) Pulse signal for the read data from the disk composing clock bits and data bits together.
(b) Fig.107 shows the timing for this signal. Leading edge of the pulse

shall be used as the reference.

(c) This signal becomes valid when all of the following five conditions are satisfied.

i) The FDD is in ready state (refer to item (12)).

ii) More than 35msec after the head loading is started.

iii) More than 18msec after the effective receival of the final STEP pulse.

iv) More than 1msec after the WRITE GATE signal becomes FALSE.

v) More than 100μsec after the level change of the SIDE ONE SELECT signal.

(11) WRITE PROTECT output signal

(a) Level signal which indicates that the write enable notch of the disk is masked.

(b) When this signal is TRUE, the data on the disk are protected from erasing and the writing of new data is inhibited.

(12) READY output signal

(a) Level signal which indicates that the FDD is in ready state.

(b) The FDD becomes ready state when all of the following four conditions are satisfied.

i) The FDD is powered on.

ii) Disk is installed.

iii) The disk rotates at more than 50% of the rated speed.

iv) Two INDEX pulses have been counted after item iii) is satisfied.

Note: Pre-ready is the state that at least one INDEX pulse has been detected after item iii) is satisfied.

(c) Required time for this signal to become TRUE after the MOTOR ON signal becomes TRUE is less than 800msec.

(d) If a hard sectored disk is used for the FDD, the above items (b)-iii), (b)-iv), and (c) cannot be applied. In such case, the ready state must be regarded as follows:

i) The FDD is powered on.

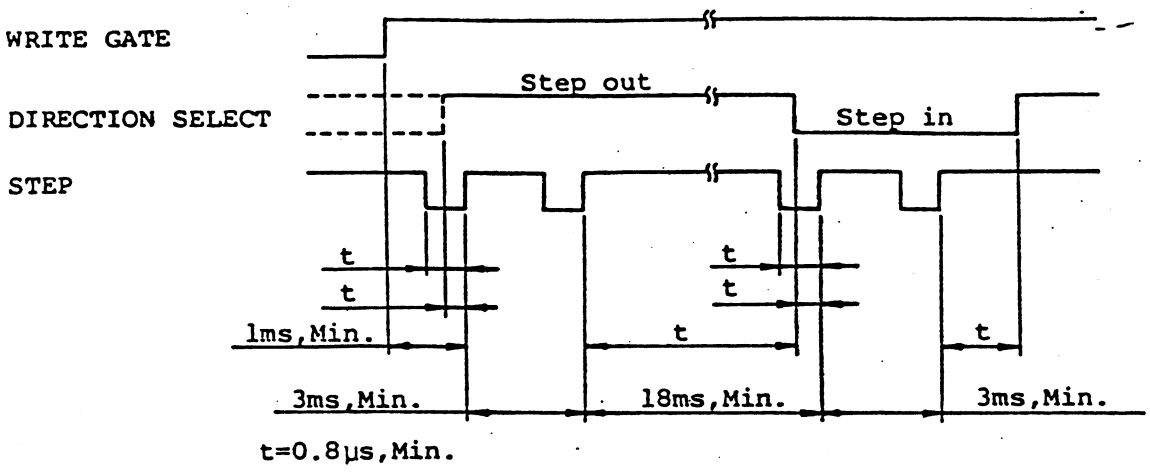
ii) Disk is installed.

iii) More than 400msec after the MOTOR ON signal becomes TRUE.

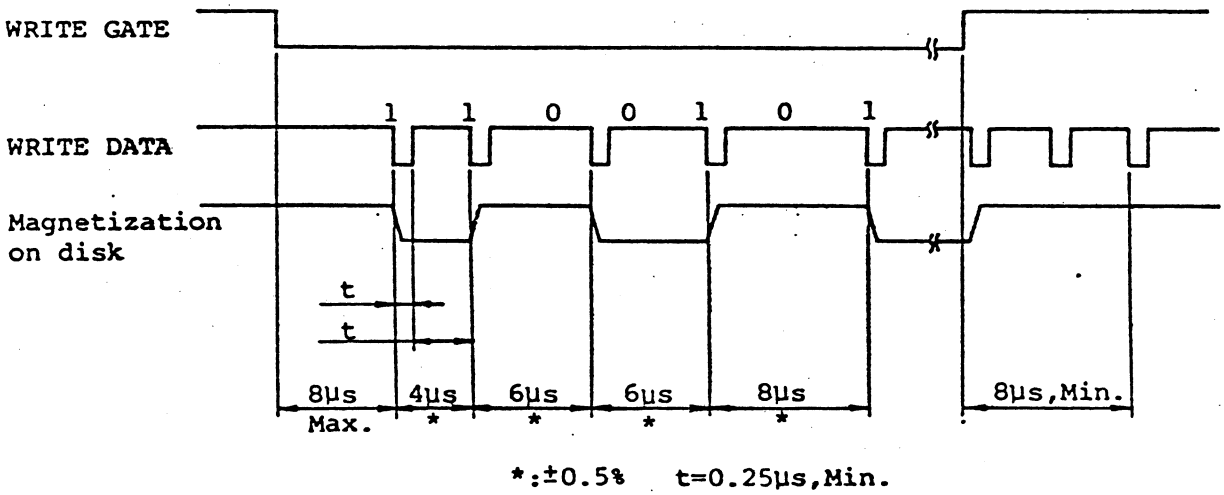
(13) IN USE input signal

(a) Level signal to indicate that all of the daisy chained FDDs are in use condition under the control of the host system.

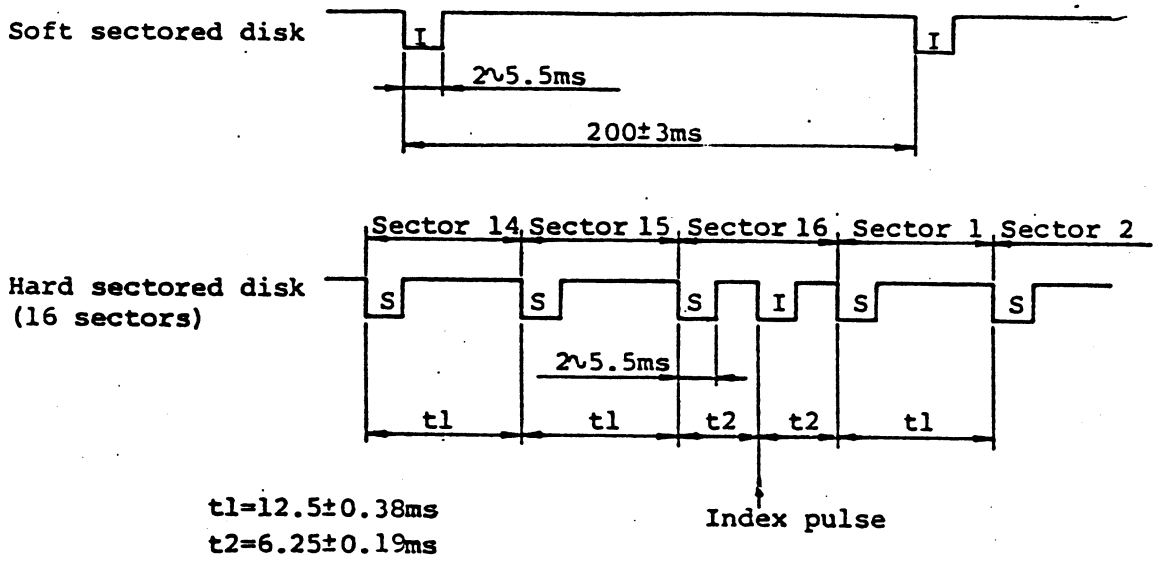
(b) The indicator on the front vessel turns on when this signal becomes TRUE.



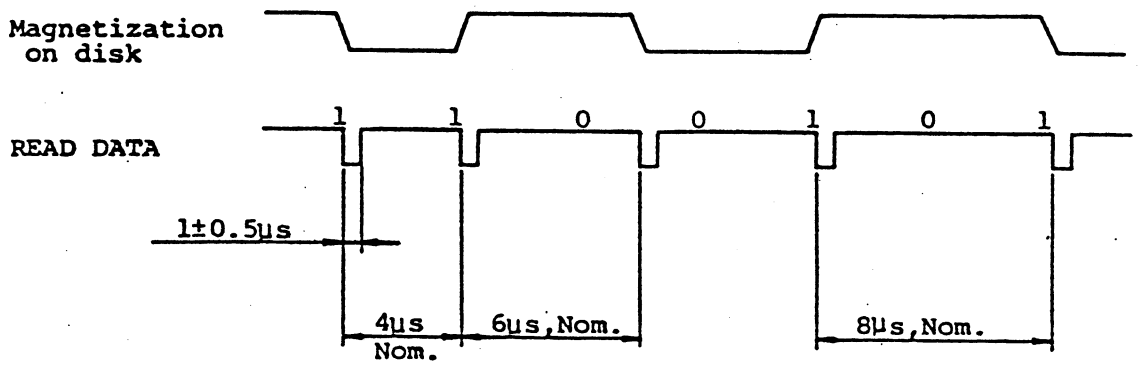
(Fig.104) STEP timing



(Fig.105) WRITE DATA timing (MFM method)



(Fig.106) INDEX/SECTOR timing



Note: The displacement of any bit position does not exceed ±20% from its nominal position.

(Fig.107) READ DATA timing (MFM method)

1-9. POWER INTERFACE

Refer to item 1-4 for power requirements.

(1) Power connector

(a) FDD side connector: AMP, Mate-N-Lock connector, P/N 172349-1 or equivalent

(b) Pin numbers: 4 pins

(c) Protection method for mis-connection: Mechanical protection by the shape of the connector housing.

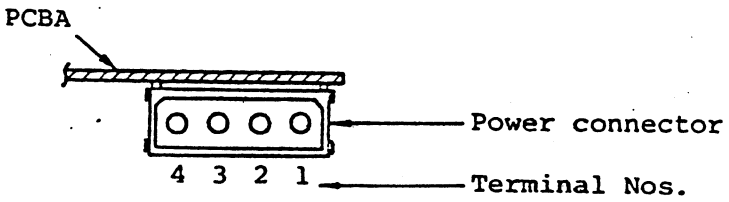
(d) Pin location: See Fig.108

(e) Power interface connections: See Table 103

(f) Cable side matched connector: AMP, P/N 1-480424-0 and pins 60617-1, or 60619-1, or equivalent

(2) Power cable

Any appropriate cables taking the maximum power consumption of the FDD and the power voltage at the connector into consideration will be acceptable.



(Fig.108) Power connector pin location (Rear view)

Voltage	Terminal Nos.
DC+12V	1
0V	2
0V	3
DC+5V	4

(Table 103) Power interface connections

1-10. FRAME GROUNDING

(1) Frame ground

(a) Frame ground is AC coupled to DC 0V by 0.01μF// 100KΩ.

(b) Insulation resistance is more than 80KΩ at less than DC 150V.

(2) Separation of the frame ground

(a) Separating method: Remove 0.01μF// 100KΩ.

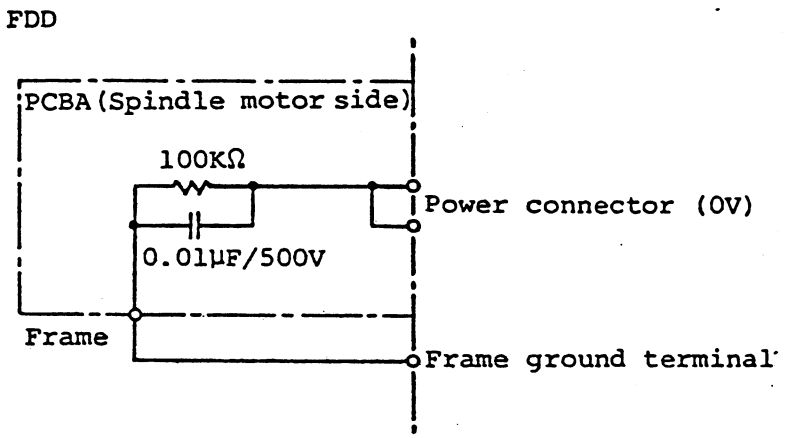
(b) Insulation resistance under separation: More than 1MΩ at DC 150V.

(c) Terminal for the separated frame ground:

Use the frame ground terminal at the back side of the FDD.

FDD side terminal: AMP faston 187 tab P/N 61761-2
or equivalent

Cable side matched terminal: AMP P/N 60972-2 or 60920-1
or equivalent



(Fig.109) Frame ground internal connection

1-11. INDICATOR AND STRAPS

1-11-1. Indicator

LED indicator on the front vessel turns on when either of the following conditions is satisfied.

(a) When the DRIVE SELECT signal of the same number as of on-state strap among DS 0 ∿ 3 straps becomes TRUE (independent of the MX strap).
(b) When the IN USE signal is TRUE.

1-11-2. Straps

All the straps are mounted on the PCB under the FDD (PCB to which the interface connector is connected). Insertion of a short bar onto the post pin of 0.64mm x 0.64mm (0.025 in) is defined as the on-state of the strap. Fig.110 shows the on-state of the straps at the shipment.

(1) MX strap

(a) The on-state of this strap is used only when the FDD is connected to the system. All the input/output signals can be effective at this time independently of the DRIVE SELECT 0 ∿ 3 signals.
(b) At the off-state of this strap, 4 FDDs, Max. can be controlled by daisy chaining.

(2) DS 0 ∿ 3 straps

(a) In the multiplex control by daisy chaining, these straps designate the address of the FDD.
(b) By the combination with the DRIVE SELECT 0 ∿ 3 signals (refer to Fig.102 and item 1-8-3 (1)), four addresses of 0 through 3 can be designated. Never designate more than 2 FDDs to a same address.

(3) HS and HM straps

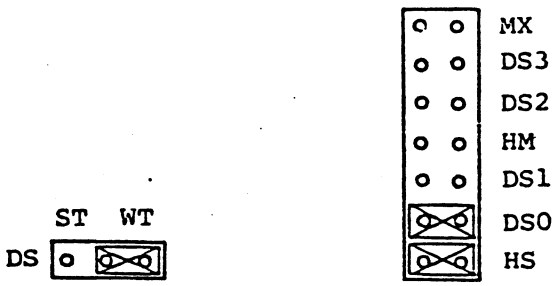
(a) Straps to determine the head load condition. Never make both of the HS and the HM straps on-state at the same time in an FDD.

(b) When the HS strap is on, head loading will be done by the DRIVE SELECT signal and the ready or pre-ready state of the FDD. (Refer to item 1-8-3, (12)).

(c) When the HM strap is on, head loading will be done by the MOTOR ON signal and after the FDD becomes pre-ready state.

(4) DS(ST/WT) strap

Strap to designate track density (48tpi or 96tpi).
WT side shall be on-state for this FDD.



Note: On-state straps at the shipment are WT, DS0, and HS.

(Fig.110) Shipping straps

Byglingsanslutningar. Kort sammanfattning.

MS	PM	HS x
DSO		DSO x
SSI	UR	DS1 x
HM	ML	HM x
DS2	IU	DS2 x
DS3	HL	DS3 x
MX	SM	MX x
	VO	
	VI	
	RE	

MX: När MX är byglad är alla drivar selectade.

DSO-DS3: Bestämmer drive-nummer. Adressera aldrig fler än två drivar på samma adress.

HS-HM: Dessa förutsätter att SM ej är byglad. Bygla aldrig HS och HM samtidigt.

MS: Laddar huvudet vid drive-select signal

MM: Laddar huvudet vid motor-on signal

IU-HL: IN use / head load in-signal

IN är byglad — IN use-signal
HL är byglad — Head Load-signal

Då ingen är byglad saknas dessa funktioner, Pin 4 är overksam. När båda är byglade har Pin 4 bägge funktionerna.

SM: Väljer HS eller HM

VO, VI och UR: Tänder lysdioden på frontpanelen. Bygla aldrig VO och UR samtidigt.

ML: Start av spindelmotorn. Då ingen bygling finns, startar spindelmotorn endast av Motor-on signalen. Vid bygling kan motorn starta dels med motor-on signal, dels då lysdioden på frontpanelen tänds.

RE: Används ej

PM: Vid bygling startar spindelmotorn automatiskt då man sätter i en diskett.